Analyzing NBTI Impact on SRAMs with Resistive-Open Defects

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***Abstract*— Density's increase in Static Random Access Memory (SRAM) has become an important concern for testing, since new types of defects that may occur during the manufacturing process are generated. In parallel, the increasing need to store more and more information has resulted in SRAMs that occupy the greatest part of Systems-on-Chip (SoCs). On the one hand, these manufacturing defects may lead to dynamic faults, considered one of the most important causes of test escape in deep-submicron technologies. On the other hand, the SRAM's robustness is considered crucial, since it may affect the entire SoC. In this context, one of the most important phenomena to degrade SRAM reliability is related to Negative-Bias Temperature Instability (NBTI), which causes memory cells' aging. In this context, the paper proposes to analyze the impact of NBTI in SRAM cells with weak resistive-open defects that can escape manufacturing test due to their dynamic behavior and, with aging, may become dynamic faults over time. The proposed combined analysis has been performed using SPICE simulations adopting a commercial 65nm CMOS technology library.**

Keywords—SRAMs; Resistive-Open Defects; NBTI

I. Introduction

Advances in nanometer technology have made possible the integration of hundred million transistors into a small area, not larger than a few square centimeters, allowing the increase of the circuits' density. In parallel, the always increasing need to store more and more information has resulted in the fact that Static Random Access Memories (SRAMs) occupy great part of the Systems-on-Chip's (SoCs') silicon area. In other words, memory has become the main contributor to the overall SoC area. The SIA Roadmap forecasted a memory density approaching 94% of the SoC's silicon area for 2015 [1].

On the one hand, the most critical downside of technology scaling beyond the 65nm node is related to the non-determinism of the devices' electrical parameters due to process variation [7][8]. This type of variation is mostly caused by random fluctuations of dopant atoms and can be observed as a fixed deviation from the device's nominal behavior [9]. Thus, technology scaling has led to the development of new types of manufacturing defects that may assume a dynamic behavior. In more detail, resistive-open defects have become one of the most significant problems in nanometer technologies, due to the ever-growing number of interconnections between layers. A resistive-open defect is defined as a defect resistor between two circuit nodes that should be connected [2]. According to [3], open/resistive vias are the most common origin of test escapes in deep-submicron technologies. Traditionally, open defects have been an area of concern, which has now moved towards weak resistive-open defects. Further, the distribution of such defects is directly correlated to the number of dynamic faults [4]. These defects generally cause timing dependent faults, which means that at least a 2-pattern sequence is necessary to sensitize them [5]. According to [4], faults requiring a large number of at-speed operations on each memory cell for sensitization are denominated dynamic faults. It is important to highlight that currently used tests are mostly designed for static faults, and do not detect dynamic faults effectively. Most of the standard March algorithms fail to detect such dynamic faults [4][6]. It poses a significant challenge to provide the detection of dynamic faults in memory cells and consequently, to guarantee the SRAM's reliability during its lifetime.

On the other hand, time-dependent deviations in the device's operating characteristics can be observed as a type of non-ideality that results from technology scaling [10]. Essentially, two sources of time-dependent deviation are identified: Bias Temperature Instability (BTI), and Hot Carrier Injection (HCI) [11]. Both are physical/chemical effects that cause a degradation of the oxide and result in a drift of the threshold voltage over time. However, BTI has become the most prominent effect as it creates interface states along the whole silicon-oxide interface. Two forms of BTI can be distinguished: Negative BTI (NBTI), which affects the pMOS transistors, and the dual Positive BTI (PBTI), affecting nMOS devices. It is important to note that the higher impact on technologies with silicon-based dielectrics is caused by NBTI and it consequently has become the most important reliability concern related to time-dependent degradation in SRAMs [9]. NBTI is defined as the effect that occurs when a pMOS is negatively biased and manifests itself as an increased threshold voltage over time. This consequently results in drive current reduction and increased noise, which in turn causes a degradation of the device's delay. The threshold's increase is estimated to be of 10-15% per year, depending on the targeted technology and its environment, while, with a smaller magnitude though, the delay degradation follows the same trend [9]. According to [12], a threshold's variation of about 10-15% per year translates into more than 10% Static Noise

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Margin (SNM) degradation after a period of 3 years, depending on the target technology and its operating conditions. Note that NBTI's effect on the long-term stability of memories expresses itself throughout the incapability of storing a value.

In this context, this paper proposes to analyze the impact of time-dependent deviations related to NBTI in SRAMs cells that have some kind of nominal behavior deviation caused by process variation associated to the manufacturing process. In more detail, the main idea behind this paper is to provide an evaluation of NBTI's impact on SRAM cells that are affected by weak resistive-open defects. These defects may have not been detected by the manufacturing test, but due to NBTI effects may cause dynamic faults in advanced phases of the SRAM's lifetime. Experimental results obtained through SPICE simulations using a commercial 65nm CMOS technology library represent a first step towards quantifying the decreasing reliability of SRAM cells affected by weak resistive-open defects over time. Reduced reliability when compared to non-defective cells has a negative impact on the SRAM's lifetime.

The paper has been organized as follows: in Section II the background related to SRAM aging is laid out and the assumed resistive-open fault model for SPICE simulations is described. Section III describes the experimental setup adopted, whereas Section IV discusses the obtained results. Finally, Section V presents the final considerations of this work.

II. Background

As previously mentioned, NBTI has emerged as one of the most important sources of permanent and time-dependent variations of the pMOS transistor's parameters, and in particular of the Threshold Voltage (V_{thp}). Indeed, process variation has led to new manufacturing defects that may generate a dynamic faulty behavior during lifetime. Thus, in this Section, the main characteristics of the SRAM cell, the NBTI effects and the fault model adopted to represent resistive-open defects in SRAM cells will be summarized.

A. The SRAM Cell

A standard six-transistor SRAM cell, composed of four transistors that form two cross-coupled CMOS inverters and two nMOS transistors that provide read and write access to the cell, is adopted in this work. The transistor sizing has been determined to be a reasonable trade-off between cell density and robustness. This choice results in the following transistor sizing values: (a) The ratio between pull-down and access transistors (Rd), where Rd = Wpull-down/Waccess = 0.20nm/0.12nm = 1.67; and (b) the ratio between pull-up and access transistors (Rp), where Rp = Wpull-up/Waccess = 0.22nm/0.12nm = 1.83. Note that these values assure the SRAM cells' stability against a noise of 200mV during read operations. Finally, the basic SRAM cell has been mapped into a commercial 65nm CMOS technology library.

B. NBTI Effects

The phenomenon of NBTI affects pMOS transistors' parameters and particularly degrades V_{thp}. In more detail, NBTI increases the V_{thp} over time and causes a shift of other electrical parameters, such as the drive current (I_{drain}) or the transconductance (*Gm*). With this intrinsic reduction of the current capability, the active pMOS transistors of the cell exhibit a progressive delay degradation called Aging. The SNM serves as a metric for the SRAM's Aging. The SNM of a conventional SRAM cell can be defined as the minimum DC noise voltage able to change the state of that cell [8]. The SNM can be computed as the side length of a maximum square nested between the two voltage-transfer-characteristic curves (i.e., for each of the back-to-back inverters) of a SRAM cell, as shown in Fig. 1.

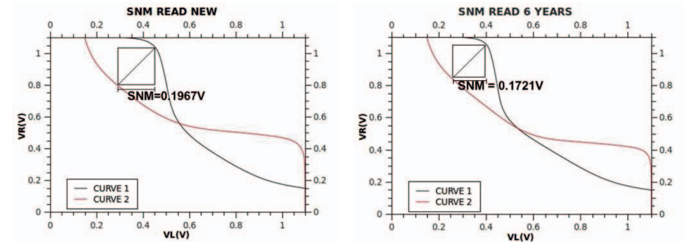

Fig. 1. Representation of SNM for a SRAM cell: New Cell and a 6-year aged cell.

Fig. 1 depicts the representation of the distinct SNMs for a six-transistor SRAM cell mapped in a 65nm CMOS technology for two situations: Fig. 1(a) depicts the SNM for a new cell, whereas Fig. 1(b) presents the resulting SNM for a 6-year-old cell. As observed in these figures, the aged cell's SNM is reduced by 12.50% with respect to the new cell's one. This means that after 6 years, such cell may suffer from bit flips during read operations for any DC noise above 0.1721 volts, instead of 0.1967 volts as for the non-aged cell [13].

The electrical model of the aging effects on a six-transistor SRAM cell assumed for SPICE simulation is depicted in Fig. 2. This model is based on the addition of a voltage source at the gate of the pMOS transistor, which needs to be aged, in series with the gate input signal. The voltage generated by this source is the ΔV_{thp}, which is added to the gate input signal. After simulating the cell for a given aging value the corresponding SNM is computed according to Fig. 1. Note that the adopted electrical model is one of many possibilities to represent aging effects on SRAM cells; direct simulation in SPICE is an exemplary viable alternative.

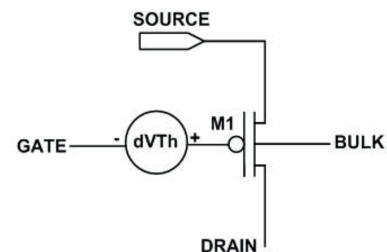

Fig. 2. SPICE model used to age a pMOS transistor by increasing V_{thp}.

C. Fault Model Associated to Resistive-Open Defects

During the manufacturing process, a standard six-transistor SRAM cell can be produced including resistive-open defects that may modify the correct behavior of the memory cell. These defects can be functionally characterized according to

the fault model presented in [15]. In more detail, this fault model represents the set of the following faulty behaviors:

- *Transition Fault* (TF): A cell is said to have a TF if it fails to undergo a transition from 0 to 1 or from 1 to 0 when it is written;
- *Read Destructive Fault* (RDF): A cell is said to have an RDF if a read operation performed on the cell changes the data in the cell and returns an incorrect value on the output. Note that this type of fault can also have a dynamic behavior, being classified as dRDF;
- *Deceptive Read Destructive Fault* (DRDF): A cell is said to have a DRDF if a read operation performed on the cell returns the correct logic value, and it changes the contents of the cell. This type of fault can also have a dynamic behavior classified as dDRDF;
- *Incorrect Read Fault* (IRF): A cell is said to have an IRF if a read operation performed on the cell returns an incorrect logic value, and the correct value is still stored in the cell.

As previously mentioned, a fault classified as dynamic is caused by a low resistive defect and demands a write operation followed by multiple sequential read operations in order to sensitize the faulty behavior [15]. The number of read operations depends on the defect size. Fig. 3 depicts the scheme adopted to model the previously described faults.

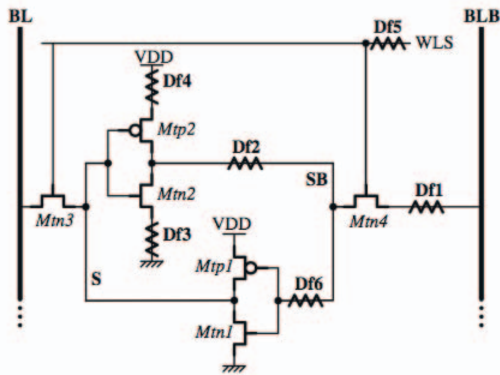

Fig. 3. Resisitive-open defects injected into a SRAM cell [15].

According to [15] TFs can be modeled using Df1, Df5 or Df6. RDF or dRDF can be observed injecting Df2, Df3, Df4, Df5 or Df6. Indeed, DRDF or dDRDF can be modeling using Df2, Df3 or Df4. Finally, IRF can be caused exclusively by Df5. It is important to highlight that the faulty behaviors associated to each defect reported in [15] differ from the ones identified in this paper. Due to the reduced defect size range adopted during the simulations, the number of faults related to each defect may not reach the complete set of faults reported in [15].

III. Experimental Setup

In order to provide the proposed analysis, electrical simulations have been performed adopting an SRAM, composed of 1024 lines of 8 columns each connected to the functional blocks, using a 65nm technological library by STMicroelectronics considering the corner defined as typical, with the temperature set to 27ºC and the voltage to 1.1V.

In order to quantify the impact of NBTI in SRAM cells with weak resistive-open defects it is necessary to perform simulations able to provide results concerning the impact of NBTI in defective as well as defect-free SRAM cells. The comparison of these results serves to understand if certain weak defects, which escape manufacturing test, reduce the reliability of the SRAM cells by causing dynamic faults over time. Note that more exhaustive simulations have to be performed in order to allow more an exact quantification of the relation between defect size and lifetime reduction.

In a first step, NBTI's impact over time has been evaluated considering a defect-free SRAM. Fig. 4 depicts the value, in *Volts*, stored in the SRAM cell over time, in *nanoseconds*, when performing the following sequence of operations: *w0r0w1r1*. Observing this figure it is possible to see that, considering the adopted experimental setup, the SRAM cell maintains the expected behavior for a lifetime of up to 20 years, since no faulty behavior is observed at logical level. However, it is possible to observe that considering 20 years of aging, the SRAM cell starts to change its behavior when *w1* is performed.

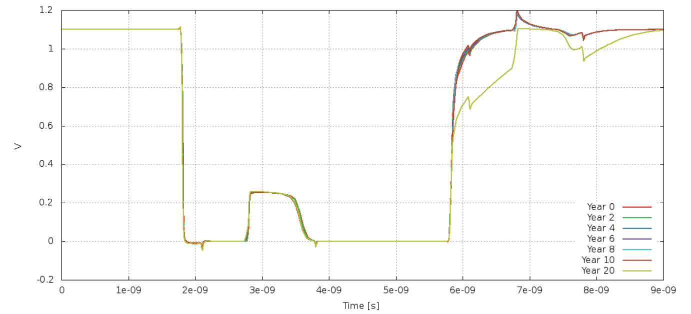

Fig. 4. Stored value (V) of the defect-free SRAM cell over time (from 0 to 20 years of aging).

Fig. 5 shows the SRAM cell output during 20 years of aging, and it is possible to see that the read value does not suffer any change over time.

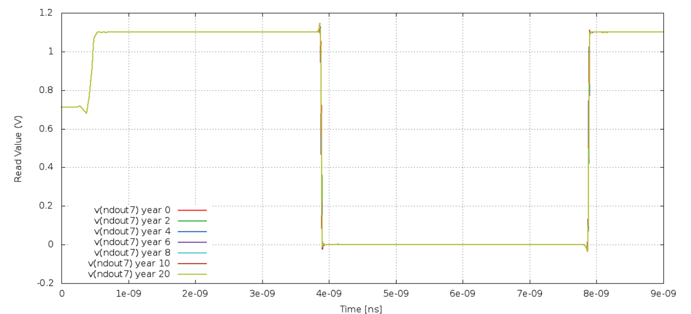

Fig. 5. Output value of the defect-free SRAM cell over time (from 0 to 20 years of aging).

Thus, the results shown in Fig. 4 and Fig. 5 demonstrate that a defect-free SRAM cell can work properly for about 20 years. Note that the functional behavior has a small change

when the cell reaches 20 years of aging (see comments related to Fig. 4).

In a second step, the relation between defect size and faulty behavior has been identified in order to understand how to simulate weak resistive-open defects. Fig. 6 summarizes the simulations performed in order to establish three distinct behaviors depending on the injected defects' size for each injection position (see Fig. 3). In more detail, it is possible to identify the following situations:

- The defect inserted in the SRAM cell is considered weak and consequently, it is not sensitize as faulty behavior;
- The defect's size generates a dynamic fault, which can be detected after a limited number of read operations, but it is not sufficient to model a static fault;
- The defect's size is sufficient to characterize a static fault in the SRAM cell.

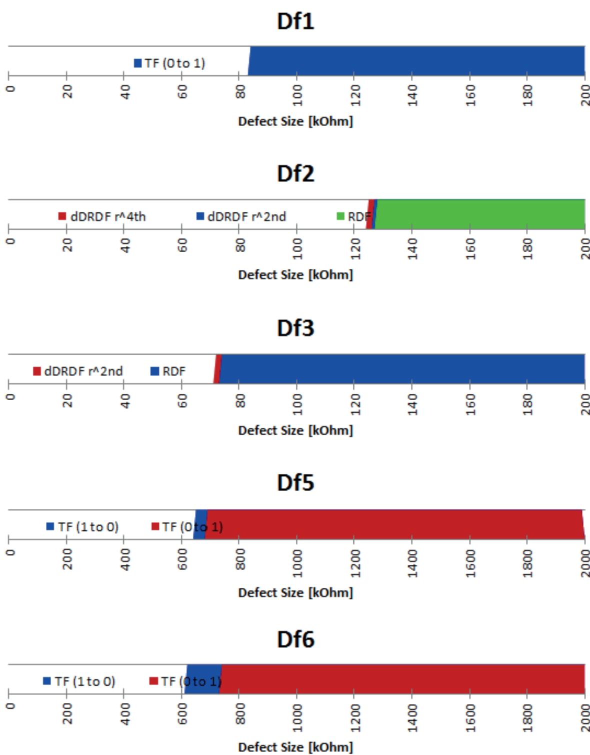

Fig. 6. Relation between defect size and faulty behaviour.

Thus, in order to better understand the impact of resistive-open defects on the SRAM cell behavior, the 6 defects have been modeled. In fact, weak resistive-open defects are directly associated to dynamic faults. Observing Fig. 6 it is possible to see the relation between resistance value and faulty behavior. Thus, depending on the resistance value, the faulty behavior observed changes between static and dynamic. Note that Df4 was left out of Fig. 6 intentionally, because it did not generate any faulty behavior considering the defect size range (from 0kOhm to 2000kOhm) adopted during the simulations. In more detail, it is possible to identify the range regarding the defect's size, which generates a specific faulty behavior for each defect position. For example, the dDRDF r^2nd is observed if a Df2 of about 127kOhm or if a Df3 of about 65-67kOhm are injected into the SRAM cell.

IV. Results

This Section summarizes the main results obtained during the simulations performed in order to provide information for the analysis proposed in this paper. The next figures depict the NBTI impact when considering SRAM cells in the presence of Df1, Df2, Df3, Df5 and Df6. In more detail, Fig. 7 to Fig. 10 show the SRAM cell's functional behavior for each defect considering different levels of aging. Due to the fact that modeling of Df1, Df5 and Df6, for the defect size range considered in this paper, did not generate any dynamic faulty behavior and that the results are exclusively associated to TF, the obtained results and their respective analysis will be presented after presenting the information related to Df2 and Df3.

Fig. 7 depicts the SRAM cell functional behavior, *Volts* over *nanoseconds*, in the presence of a Df2 equal to 115kOhm. This value has been selected considering that a Df2 equal or bigger than 125kOhm is able to sensitize the fault at logic level, is being classified as dynamic for a defect from 125kOhm to 127kOhm and as static fault for a defect equal or bigger than 128kOhm. Thus, the value of 115kOhm is within the defect size range that may not be sensitized at logic level, which means that no faulty behavior can be observed during read and write operations. Observing Fig. 7 it is possible to see that after 2 years of aging, a *w1* operation followed by 7 read operations changes the value stored inside the cell to 0 (dashed circle). Indeed, it is possible to observe that after 3 years of aging only 1 read operation is necessary to sensitize the faulty behavior (dotted circle).

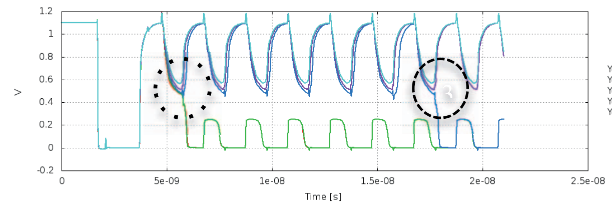

Fig. 7. Faulty behavior: stored value (V) related to Df2.

Fig. 8 depicts the output value of the SRAM cell. In this figure it is possible to observe that the read value changes when the SRAM is aged.

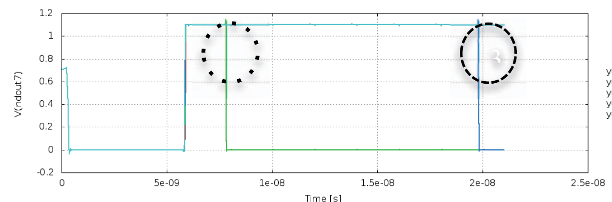

Fig. 8. Faulty behavior: output value (V) related to Df2.

In more detail, it is possible to identify that after 2 years of aging, as the stored value changed from 1 to 0 after 7 read operations, the value read from the cell would be 0 (dashed circle). This characterizes the occurrence of a dRDF. A similar behavior is observed after 3 years with the difference that the dRDF is observed after only 1 read operation (dotted circle). This means that a SRAM cell with a weak resistive-open defect that, since it is not able to sensitize the faulty behavior at logic level, eventually escapes manufacturing test can become a source of faulty behavior when the cell is affected by NBTI during lifetime. Considering the specific case reported in Fig. 7, it is possible to conclude that a cell with a weak defect of 115kOhm will operate properly only up to 3 years compared to at least 10 years estimated considering a defect-free SRAM cell.

Fig. 9 depicts the relation between defect size and faulty behavior considering Df2 after 3 years of aging. It is possible to see that the first faulty behavior can be observed with a defect of around 112kOhm, dDRDF r^4th, the second with a defect around 113kOhm, dDRDF r^2nd, and finally, the static RDF is observed with a defect size bigger than 115kOhm.

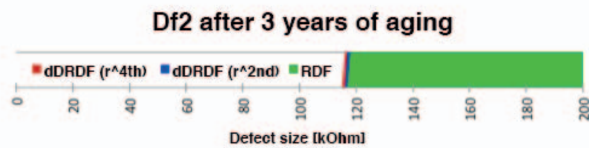

Fig. 9. Relation between defect size and faulty behavior considering the Df2 after 3 years of aging.

The results obtained considering the Df3 with a value of 60kOhm are plotted in Fig. 10. Observing this figure it is possible to see that after only 1 year of aging the faulty behavior can be sensitized performing 4 consecutive read operations (dashed circle). Note that this value is reduced to 3 operations after 2 years of aging (dotted circle).

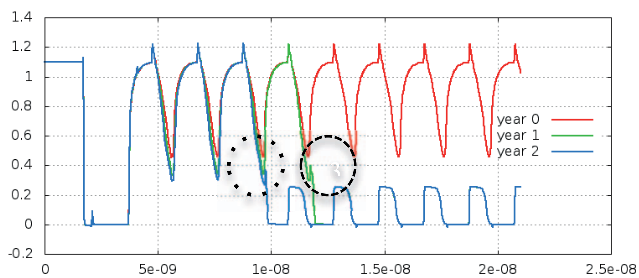

Fig. 10. Faulty behavior: store value (V) related to Df3.

In Fig. 11 it is possible to see the output value for the SRAM cell with a Df3. For this defect, it is possible to drawn a similar conclusion than the one related to Df2.

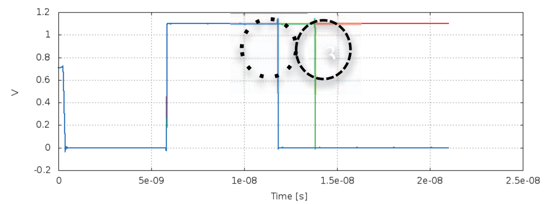

Fig. 11. Faulty behavior: output value (V) related to Df3.

As previously mentioned, Df1, Df5 and Df6 are going to be analyzed together, because they generated similar faulty behaviors during the performed simulations. Basically, these three defects, considering the defect size range adopted in this paper, generated only TFs. More specifically, the simulations performed have only been able to distinct between ranges where a TF is propagated to the logic level or not. Note that TFs do not possess any dynamic faulty behavior, since they are defects that are associated to write operations exclusively. In more detail, for Df1, a TF from 0 to 1 is observed when a defect equal or bigger than 84kOhm is present. Note that a TF from 1 to 0 has not been sensitized during the simulations related to Df1. However, for Df5 this value has to be equal or bigger than 700kOhm for a TF from 0 to 1 and equal or bigger than 660kOhm for a TF from 1 to 0. Considering Df6, these values change to 740kOhm for a TF from 0 to 1 and to 620kOhm for a TF from 1 to 0.

The simulations of Df1, Df5 and Df6 generated results that differ from the expected ones. In more detail, it was observed that the defect size necessary to sensitize a TF increases with aging. This characterizes the opposite behavior with respect to the one observed for Df2 and Df3. Thus, while an SRAM cell with Df2 or Df3 possess a range of not detected faults that with aging become a reliability problem, the range of not detected defects of SRAM cells with Df1, Df5 or Df6 never will generate faults. Consequently, the latter group of cells possesses a range of faults that would be detected and, after a certain time of aging, are not causing faulty behavior anymore. An example is given in Fig. 12, where the faulty behavior observed during the first three years, changes to fault-free behavior after 4 years of aging. Thus, as the necessary defect size already is within the range of detectable defects, the defect size values for Df1 from 0 to 83kOhm does not represent a reliability issue for SRAMs.

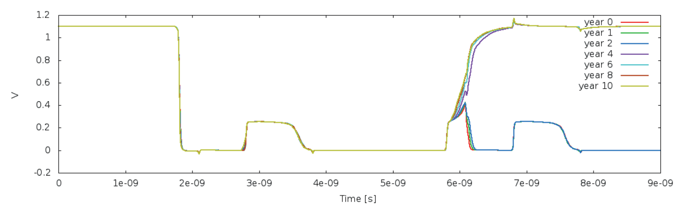

Fig. 12. Faulty behavior: store value (V) related to Df1.

The two opposite effects of aging are depicted schematically in Fig. 13.

Fig. 13. Scheme for faulty behavior before and after aging.

V. Final Considerations

This paper presents an analysis of the NBTI impact on SRAM cells with weak resistive-open defects that may escape manufacturing tests. The main reason for the proposed analysis is associated to the fact that certain weak resistive-open defects, which are not propagated to the logic level, over time may present faulty behavior due to the SRAM's aging. In other words, defects that initially did not represent a reliability problem, because they are not able to sensitize any faulty behavior and were considered to be weak, may become a source of faults after the cell was affected by NBTI.

Regarding Df2 and Df3, it is possible to conclude that NBTI may generate a faulty behavior associated to a weak defect that did not sensitize any faulty behavior before aging and consequently may escape manufacturing testing.

However, for Df1, Df5 and Df6, aging caused an opposite behavior, meaning that when the cell is affected by NBTI, the defect size value necessary for sensitizing the faulty behavior at logic level has to be even bigger than the one necessary for sensitizing the faulty behavior in a non-aged cell.

Acknowledgment

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