Ionizing Radiation Effects on a COTS Low-Cost RISC Microcontroller

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***Abstract* — Electronic systems functionality degrades when these systems are operating in harsh environments such as those where they are exposed to ionizing radiation. Understanding and measuring these effects is extremely important in order to design systems that can operate reliably. This work discusses experimental data of heavy ion and x-ray radiation effects on a Commercial-Off-The-Shelf (COTS) low-cost microprocessor. The heavy ions test results suggest that, in this technology, the SRAM is more sensitive to SEE than flash memory. Ions with a LET higher than 5 MeV/mg/cm² may disrupt the device's proper operation.**

***Index Terms*— SEE, TID, transient response, x-ray, radiation effects, COTS microprocessor.**

I. INTRODUCTION

Digital systems are often used in space applications to process data, implement control logic, or even store data from sensors. These systems are composed of electronic devices, such as microcontrollers and microprocessors, which may be exposed to higher levels of ionizing radiation when operating in space. The main effects of ionizing radiation on electronic devices are Single Event Effect (SEE), Displacement Damage (DD), and Total Ionizing Dose (TID) [1- 7]. These effects can be of a reversible or irreversible nature, but all devices exposed to ionizing radiation are damaged to some extent, owing to the accumulated radiation dose.

Many digital systems used nowadays have a Reduced Instruction Set Computer (RISC) architecture. In the chosen device, model M0+ data processing occurs only on register contents and the addressing mode is determined by register contents and instruction fields.

ARM (Advanced RISC Machine) processors present a good balance of performance, cost, and power consumption [8]. There are space-grade versions of these devices that can be used in harsh environment applications, but these versions are much more expensive than commercial and industrial devices. A Commercial-Off-The-Shelf (COTS) version of this processor can be used to perform auxiliary computation and minor tasks, and due to their reduced cost, easy availability and good performance, it is extremely important to test these COTS devices in harsh environments [9]. In this work, an ARM Cortex M0+ COTS was tested for its tolerance regarding Single Event Upset (SEU) and TID.

II. DEVICE UNDER STATIC TEST

The device chosen was the MKE02Z64VQH4, produced by NXP Semiconductors. It has an ARM Cortex-M0+ core, which runs at up to 20 MHz and operates at a supply voltage of 3.3 V. Although the fabrication of ARM processors has been reported for tech nodes down to 55 nm [10], the commercial devices are probably produced in the range of 130 to 180 nm. The device has 64 kB of flash memory, which is used to store the program, and 4 kB of SRAM, which is used to store variables and some volatile data. Additionally, the device has many peripherals, such as Universal Asynchronous Receiver/Transmitter (UART), Serial Peripheral Interface (SPI), General-Purpose Input/Output (GPIO), Pulse-Width Modulation (PWM) outputs, Analog-to-Digital Converters (ADC) and many others. The non-volatile flash memory has an Error Correction Code (ECC) algorithm embedded that can resolve single bit faults and detect double bit faults. These features make the device interesting for minor tasks and co-processing applications in harsh environments.

The microcontroller was mounted on a development board model FRDM-KE02Z produced by NXP. This development board has an Onboard Serial and Debug Adapter (OpenSDA) which is used to debug the microcontroller program and to communicate with the device on a serial interface. Using the ARM Debug Access Port (DAP), the debugger can read the status, registers, and access the flash and SRAM memories [8, 11]. Fig. 1 shows the overall architecture of the ARM Cortex-M0+ core.

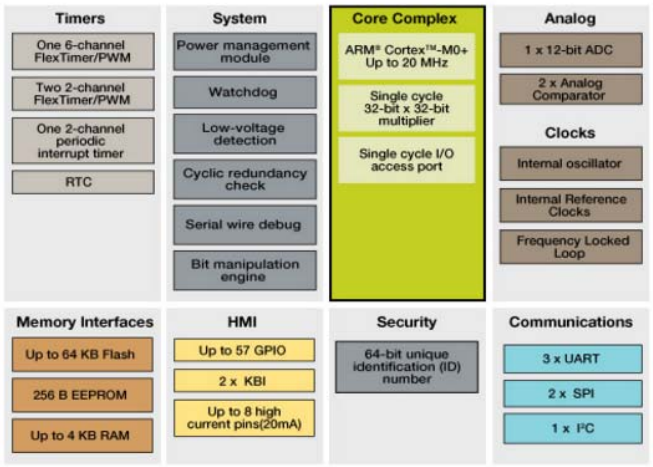

Fig. 1. MKE02Z64VQH4 device's architecture. [10]

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III. METHODOLOGY

The main goal of the experiment was to characterize an ARM Cortex-M0+ processor with respect to TID and to SEU. In this process, emphasis is given on understanding the flash and SRAM embedded memories reliability and degradation in harsh environments. In order to estimate the accumulated dose on the device under test (DUT) due to X-ray radiation, and to allow the heavy ions to reach the sensitive volume of the DUT during SEU test, the packaging epoxy layer was removed by a chemical process. Fig. 2 shows a picture of the DUT, after epoxy removal.

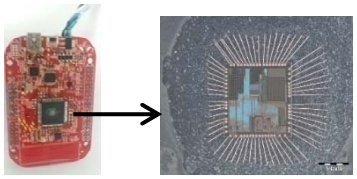

Fig. 2. Test board (left) and DUT detail without epoxy layer (right).

The device was irradiated using two different sources: heavy ions in the Universidade de São Paulo 8UD Pelletron accelerator and 10-keV X-Rays in the Shimadzu XRD-7000 X-Ray Diffractometer at the Centro Universitário FEI [5,12-14].

To assess the effects of ionizing radiation on the DUT, a dedicated application program was developed to read/write the contents of each memory space (flash and SRAM). The memory was accessed through the Debug Access Port of the DUT and saved in files for further analysis in order to compute the event rate. In the beginning of each irradiation procedure, the flash and the SRAM memories were programmed with five different patterns:

- The memory array was filled with 0x00H.
- The memory array was filled with 0xFFH.
- The memory array was filled with 0xAAH.
- The memory array was filled with 0x55H.
- The memory array was filled with random numbers.

Then, the CPU executed the application code and it was halted when one of the two following conditions was satisfied: (A) a certain predetermined number of particles has already hit the DUT or (B) a certain predetermined dose has been accumulated. The flash and the SRAM memories were read out and the number of bit-flips in each memory region is computed. The reason why the CPU was halted is to reduce the effect of dead time (the time taken by the CPU to run some instructions). The flowchart of this software can be seen in Fig. 3.

A - Experimental Setup for SEE test

In order to measure the sensitivity of the microprocessor to errors due to SEU, the 8 UD Pelletron accelerator located on *Laboratório Aberto de Física Nuclear* of the Universidade de São Paulo (LAFN-USP) was used. In this setup, a low intensity flux of particles (protons and heavy ion beams) in-vacuum is obtained, using Rutherford scattering in a gold foil [13]. In Fig. 4, the DUT inside the vacuum chamber is shown.

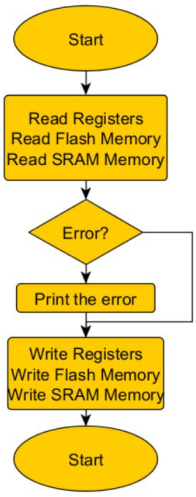

Fig. 3. Flowchart of the SEE checking software.

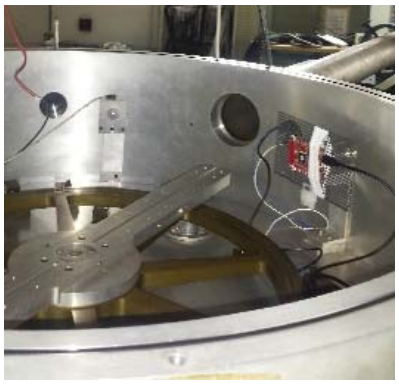

Fig. 4. Scattering chamber for heavy ions irradiation at 8 UD Pelletron Accelerator.

The penetration range of the particles inside a material depends on the particle energy and the linear energy transfer (LET), which is determined mainly by the atomic number of the incident particle. The maximum value of the particle LET in the material is known as the Bragg peak. A few millimeters already completely prevent the particles from passing through the epoxy and reaching the sensitive parts of the device [12-14]. In order to evaluate the minimum range of the particle and determine the sensitive area of the DUT, ^{12}C beams with three different LET were used in unpackaged DUT: 2.4, 2.9 and 3.2 MeV/mg/cm^2. ^{16}O and ^{28}Si ion beams with 5.0 and 12.3 MeV/mg/cm^2, respectively, were also used to extract the SEU cross-section.

B - Experimental Setup for TID test

The X-ray irradiation procedures were performed with a Shimadzu XRD-7000 Diffractometer, with a 96 rad/s dose rate. X-ray sources are very versatile for studying radiation effects in electronic devices since it is possible to modify the X-ray tube current and the source-device distance, in order to choose an adequate dose rate. This source is more secure than Co-60 irradiators since the X-ray radiation is present only inside the Diffractometer, which can be turned off

immediately [12, 14]. A voltage of 20 kV was applied on the X-ray tube terminals, generating an X-ray beam of 10 keV. The effective energy was measured using aluminum foils of different thickness and calculating the half–attenuation of the Al layer [5,12]. In fact, for TID effects, 10-keV X-ray radiation is a very convenient source of radiation owing to its higher charge yield compared to protons, alpha particles and heavy ions [12,14,15]. The correlation between X-ray and proton radiation-induced degradation has been observed for proton energies from 20 to 200 MeV and also in the radiation-induced degradation of field oxides in bulk-silicon technologies [16]. 10-keV effective energy X-rays are very convenient for studying radiation effects in electronic devices since these photons generate secondary electrons with a range of the order of 500 nm, which is comparable to the transistor field oxide thickness. The effects generated by these photons are comparable also to the effects provoked by Co-60 gamma sources [12, 14-16].

The DUT was placed 10 cm away from the X-ray beam source, to ensure field radiation area homogeneity. In this position, the X-ray beam covers an area of about 2.0 x 2.0 cm^2, which is much larger than the sensitive device area. The dose rate was calibrated by measuring the exposure using an ionization chamber, and the X-ray dose rate in silicon was estimated using air and silicon mass attenuation coefficients [5,12]. The device's supply current was measured during the irradiation process by a National Instruments NI-PXIe-1062Q electric characterization system, in order to verify the device degradation due to cumulative total ionizing dose effects [12].

IV. Experimental Results and Discussion

A - SEE Experimental Results

During the ^{28}Si and ^{16}O heavy ion irradiation, SEL (Single Event Latch-up) errors were observed, which caused the debug apparatus, i.e., the JTAG logic to stop working. Therefore, it was impossible to read out the memories of the DUT, which indicates that this ARM COTS do not tolerate LET values higher than 5.0 MeV/mg/cm^2. Since heavy ion beams provoke transient faults, resetting the system after each SEU was enough to recover its functionality. On the other hand, with ^{12}C ion beam with LET values below 3.2 MeV/mg/cm^2, the debug circuitry worked perfectly and some bit-flips in the SRAM memory could be observed. Owing to the high complexity and high-density circuitry of the core, it was not possible to pinpoint the reason why it stopped communicating with the debug port. During the ^{12}C ion irradiation, no SEL was observed and the number of errors (SEU) in the SRAM and flash memories could be measured.

The SRAM bit cross-section versus LET is shown in Fig. 5. Different LET values are achieved using different energies for the same ^{12}C ion beam. This plot suggests that the SEU bit-flip cross-section is practically constant for this DUT. In Table 1 the ^{12}C LET values, the flash and SRAM bit-flip cross-section, and the ion range inside the DUT sensitive volume are shown. The SRAM bit-flip cross-section was calculated based on an average number of bit-flips for all the patterns, since that a significant variation was not seen among the patterns. The constant bit-flip cross-section behavior indicates that the ion beam passed through the DUT sensitive volume even in the lower ^{12}C range of 28.4 μm. The range for the heavier ions (^{16}O and ^{28}Si) is enough to traverse the sensitive volume. Summarizing, the device could not cope with heavy ions with LET higher than 5 MeV/mg/cm^2. The non-occurrence of bit-flips in the Flash memory suggests a much higher tolerance to heavy ions than SRAM. However, the lack of bit-flips observations in the flash memory may be due to the ECC's action. No upsets were seen in registers during the experiments using ^{12}C ions.

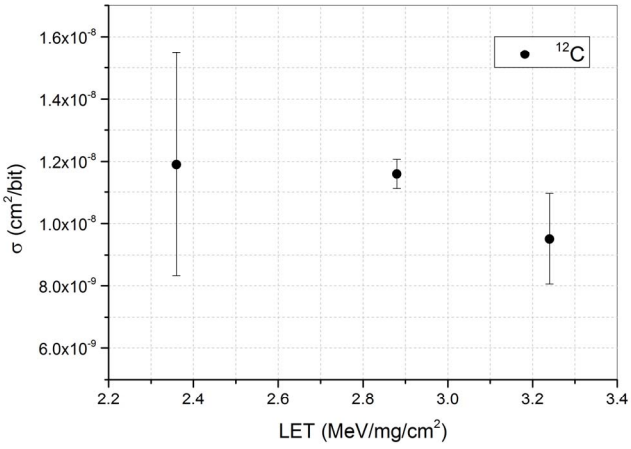

Fig. 5. SRAM bit cross-section as a function of LET.

TABLE 1. Bit cross-section for flash and SRAM memories as a function of ^{12}C LETs and the ion range in the DUT.

LET (MeV/mg/cm²)	*Flash σ (cm²/bit)*	*SRAM σ (cm²/bit)*	*Range (μm)*
2.4 (^{12}C)	0	1.2(4)x10^{-8}	61.0
2.9 (^{12}C)	0	1.16(5)x10^{-8}	38.2
3.2 (^{12}C)	0	9.51(14)x10^{-9}	28.4
5.1 (^{16}O)	SEL	SEL	22.0
12.3(^{28}Si)	SEL	SEL	28.4

B - TID Experimental Results

For the X-ray irradiation, we did not observe DUT functional disruption up to 30 krad(Si). On the other hand, after 60 krad(Si) of accumulated dose, the processor entered in *secure device mode* and it was unable to reprogram the memories. The flash module of the device has a security feature, which is configured by the first two bits of the Flash Security Register [11]. This information suggests that these bits were influenced by the X-ray cumulative dose [12]. Additional dynamic tests will be performed in the near future in order to confirm the register sensitivity to X-ray radiation and to verify the device tolerance to ionizing radiation.

In Fig. 6, a plot of supply current as a function of time is presented. Time is correlated with accumulated dose through the 96 rad/s dose rate. It is worth commenting that, during irradiation up to a dose of 60 krad(Si), significant changes in

supply current were not observed, except when programming the memories. That is, there was no change in this current due to effects of trapped charges.

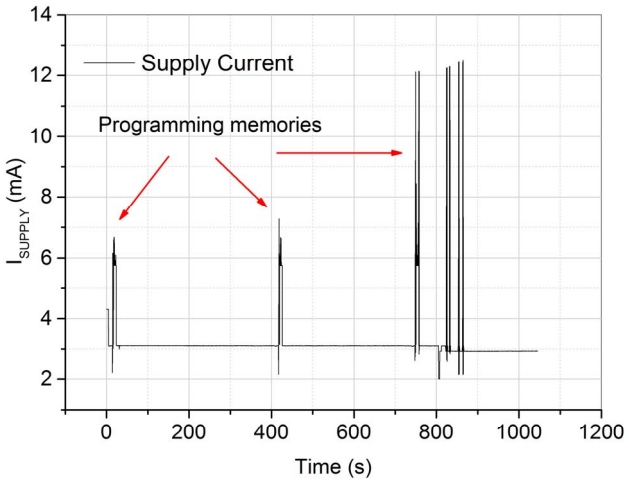

Fig. 6. Supply current as a function of time during X-Ray irradiation using 96 rad/s.

V. Conclusions

In this work, static test data regarding ionizing radiation with heavy ions and 10-keV X-ray on an ARM Cortex-M0+ processor was preliminarily described. SRAM and flash memories were monitored during the irradiation procedures. Due to the high circuit complexity, it was not possible to determine exactly how and where the single-event effect occurred. It is only possible to verify the consequences these effects provoked on the circuit, such as errors in the SRAM memory space and a possible latch-up observed on the device. The heavy ion irradiation results suggest that the SRAM is much more sensitive to SEE than flash memory. It was not observed any difference in the number of bit flips due to different programmed pattern used in these tests. Moreover, ions with LET higher than 5.0 MeV/mg/cm^2 caused the device to stop functioning (system crash) and the communication with the debug circuitry also failed, requiring power cycling to restore normal operation. Finally, as observed, X-ray radiation accumulated on the processor beyond 60 krad(Si) forces it to enter in the *secure operating mode*, preventing the user from accessing the flash memory.

Acknowledgment

This work has been supported in part by Centro Universitário FEI, and Centro de Tecnologia da Informação Renato Archer and the Brazilian research funding agencies FAPESP, FINEP (Projeto CITAR), and CNPq.

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