An Early Prediction Methodology for Aging Sensor Insertion to Assure Safe Circuit Operation due to NBTI Aging

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***Abstract*—This paper proposes an early resilience methodology to identify circuit output nodes where aging sensors should be inserted for an error prediction framework. The methodology is based in a pre-layout statistical estimation of the signal paths likely to become critical due to NBTI and/or Process Variations. To handle the fact that spatial correlation information is not available at early steps of the design flow, a statistical approach maximizing critical paths coverage is proposed. The results obtained with the early prediction methodology are compared with those obtained with spatial correlation information. The proposed methodology provides a good prediction of the set of critical paths to be monitored. Furthermore, location and number of aging sensors required to be inserted at critical paths output nodes are closely predicted.**

I. Introduction

Negative Bias Temperature Instability (NBTI) is a major reliability concern in nanometer technology nodes [1]. NBTI gradually increases PMOS threshold voltage (V_{th}) over time, which translates into an increase of circuit delay. Due to NBTI effect, a circuit may fail its timing specification before the expected lifetime. Therefore, the impact of NBTI on circuit delay needs to be considered early in the design phase to assure circuit correct functionality over the entire lifetime.

The error prediction technique [2] allows to counteract NBTI by performing corrective actions like to decrease clock frequency, to increase supply voltage, and to redistribute computer tasks, before a faulty behavior occurs. Aging sensors [2][3][4][5][6] are inserted at circuit output nodes to keep under surveillance delay degradation and to detect if corrective actions are needed. However, the aging sensors insertion can introduce a large power and area overhead for large circuits. Therefore, the error prediction technique requires a cost−effective methodology to shorten the number of aging sensors to be inserted while critical paths coverage is assured. Moreover, to make the error prediction technique suitable to be applied in a conventional design flow, critical paths identification and the aging sensors insertion should be performed at early steps of the design flow.

In [7] aging-aware Static Timing Analysis is performed to identify the critical paths set. However, NBTI effect strongly interacts with process parameters variations producing shifts on both the mean and the variance of circuit timing responses [8]. Therefore, static timing analysis (even considering NBTI effect) may lacks of accuracy.

In [9] and [10] the effect of process variations in the critical paths selection procedure has been considered by performing Statistical Static Timing Analysis (SSTA). Those approaches require gates placement information to compute spatial correlation between process parameters. However, this information is not usually available at early design stages. Other statistical approach is proposed in [11]. A small set of representative critical paths is selected to be monitored and to statistically infer the aged delay of a larger set of critical paths. Although this approach allows to reduce the required number of aging sensors to be inserted, uncertainties introduced by process variations and aging may require to be considered.

For timing prediction early in the design flow, SSTA approaches using correlation bounds becomes atractive. Approaches in [12][13] compute bounds for the circuit delay distribution, but this is not the concern here. In an error prediction framework the aim is to minimize the probability that a critical path affecting circuit reliability is unmonitored.

This paper proposes an early prediction methodology to identify the circuit output nodes where aging sensors should be inserted for an error prediction framework. The combined effect of NBTI and process variations is considered. A statistical approach maximizing path coverage is proposed to cope with the unknown spatial correlation information. The results show that our approach allows to identify most of the critical paths and nodes to be monitored at the early design stages.

The rest of this paper is organized as follows: Section II presents the NBTI statistical model and the maximum path delay degradation criterion used in this work. Section III presents an overall description of the proposed methodology for cost-effective aging sensor insertion. Section IV presents our approach to select the critical paths set without availability of spatial correlation information. Section V presents the results and the validation of the proposed methodology in some ISCAS85 benchmark circuits. Finally, Section VI presents the conclusions of this work.

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II. NBTI PHENOMENOM AND MAXIMUM DEGRADATION CRITERION

A. NBTI Impact in Threshold Voltage

NBTI phenomenom occurs in PMOS transistors biased in inversion. During the stress condition, $Si - H$ bonds at the gate oxide-channel interface are broken, leaving unsatisfied bonds that act like hole traps. When stress condition is removed, a partial recovery of interface traps take place. As a result, NBTI gradually increases V_{th} of PMOS devices along life operation. NBTI effect is aggravated in scaled CMOS, due to higher electric fields and higher temperatures [14]. The amount of V_{th} shift due to NBTI depends on time, technology parameters, supply voltage, temperature and stress probability, which can be defined as the average time the device is at stress condition. A simplified model that accounts for process variations and NBTI effect in V_{th} was proposed in [15]:

$$\Delta Vth_{NBTI} = (1 - S_v \cdot \Delta Vth_{PV}) \cdot A \cdot \alpha^n \cdot t^n \quad (1)$$

where A and S_v are fitted constants related to technology and operation conditions, ΔVth_{PV} is the initial variation in V_{th} due to process variations, α is the stress probability and n is a constant with a value of $1/6$. It should be highlighted that ΔVth_{PV} is composed of both correlated and independent (due to Random Dopant Fluctuations) variations.

The total ΔV_{th} a device may experience is obtained by adding the contributions of process variation (ΔVth_{PV}) and aging due to NBTI (ΔVth_{NBTI}). After rearranging the terms the following expression is obtained [15]:

$$\Delta V_{th} = A \cdot \alpha^n \cdot t^n + (1 - S_v \cdot A \cdot \alpha^n \cdot t^n) \cdot \Delta Vth_{PV} \quad (2)$$

It can be observed at $t = 0$ that total ΔV_{th} is due to process variation only. However, as time increases the first term increases the V_{th} mean value, while the second term indicates the rate of V_{th} degradation is reduced over time.

B. Maximum Path Delay Degradation Criterion

For a signal path, its delay degradation depends on the specific ΔVth of each device activated for the performed transition. However, devices stress probabilities (α) are hard to be estimated for random logic circuits, because the specific circuit workload is unknown. A maximum path delay degradation criterion is assumed to assure a conservative analysis for the early resilience methodology.

The worst case stress probabilitiy at the main input of a path, which produces the maximum delay degradation can be found as shown in [16]. Consider the five inverter chain of Figure 1. The α value at the path input (α_{in}) to obtain its maximum delay degradation should set α maximum at each activated PMOS transistor along the chain. Thus, a low value of α_{in} (0.1 in our work) is considered for the 0 to 1 transition at the path input, and a high value of α_{in} (0.9 in our work) is considered for the 1 to 0 transition at the path input. It should be highlighted that in this work the worst case value of α_{in} was found for each single path transition (t_{plh} or t_{phl}).

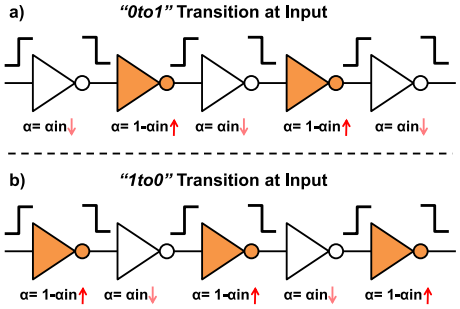

Figure 1. Stress probability conditions for worst case degradation

III. GLOBAL METHODOLOGY FOR AGING SENSOR INSERTION

Figure 2 shows the flow diagram of the early prediction methodology to identify the set of paths and nodes to be monitored. The input file is the circuit netlist at gate level (Pre-Layout Level). Path pre-filtering using static timing analysis based on process corners is performed. A coarse selection condition is used to define the set of pre-filtered paths. This allows to reduce the overall topological paths set in a reasonable amount of computational time. Then, the set of pre-filtered paths is analyzed with SSTA. Two statistical selection criteria are evaluated to identify the paths likely to become critical due to NBTI and/or Process Variations. Once the set of critical paths is obtained, the output nodes (primary outputs) of these paths are identified. The aforementioned methodology has been implemented in C++ code. In the following, a more detailed description of each step in the proposed methodology is given.

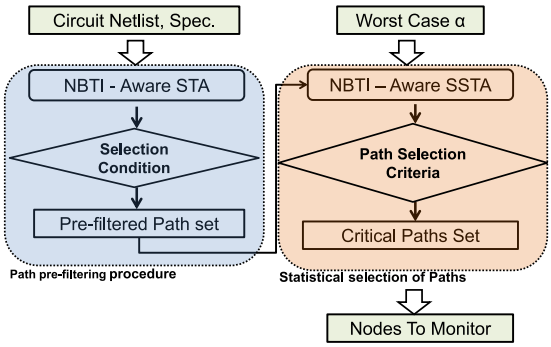

Figure 2. Flow diagram of the proposed early prediction methodology

A. Path pre-filtering

Figure 3 illustrates the path pre-filtering step, which allows to identify those paths having certain probability to become critical in a reasonable amount of computational time. The paths are ranked according to their nominal delay values as P_1, P_2, P_3, P_4, where P_1 states for the Longest Critical Path (LCP) and P_4 represents the path with the shortest delay. Delay information of each path using Fast-Fast (FF) and Slow-Slow (SS) process corners are obtained by Static Timing

Analysis. The time delay of $P1$ at FF corner (D_{FF1}) is taken as the delay threshold to obtain the *pre-filtered paths set*.

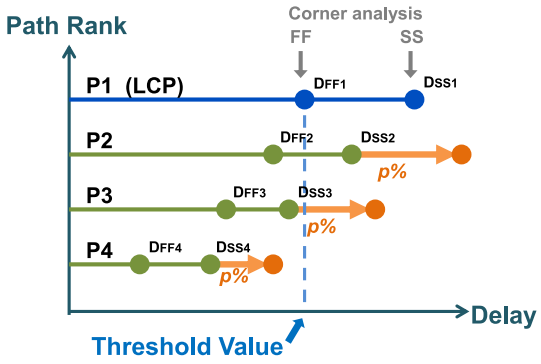

Figure 3. Path pre-filtering procedure.

Selection condition for path-prefiltering: a path is selected, if its delay in the SS corner (D_{SS}) plus some worst case percentage of aging degradation ($p\%$) is greater than the delay threshold value: $D_{SS}(1+p\%) > D_{FF1}$. Paths that met this condition could exhibit a delay greater than the LCP delay during operational lifetime.

As can be seen in Figure 3, $P2$ and $P3$ meet previous condition, then those paths are included in the pre-filtered path set. On the other hand, $P4$ does not take delays greater than the LCP delays under any process corner and any aging condition. Then, $P4$ does not require to be further analyzed. In this work, a maximum possible percentage of degradation $p = 20\%$ is assumed [17]. This conservative value of possible aging degradation assures that any path endangering correct circuit operation will not be left out.

B. Statistical Identification of Paths to be monitored

The pre-filtered paths set is next analyzed using SSTA. Gate delays are modeled as linear functions of process parameters. Variations in channel width, channel length, oxide thickness and threshold voltage have been considered. Applying properties of linear models, paths delays distributions and covariance between them can be computed.

*1) **Statistical Selection Criteria**:* A Statistical Selection Criteria allows to shorten the number of paths that really need to be under surveillance. In such way, the number of aging sensors to be inserted is minimized while critical paths coverage is assured. The two following statistical criteria are proposed to establish whether a path should be monitored.

Criterion 1: The first criterion establishes that a path should be monitored if under NBTI and Process Variations effects (at $t = 10$ years) its probability to have delays greater than the LCP delays without aging (at $t = 0$ years) is greater than an user-defined threshold (ε),

$$P(D_{i,a} > D_{LCP,f}) > \varepsilon \tag{3}$$

where $D_{i,a}$ stands for the delay distribution of the path under analysis (taken from the pre-filtered paths set), and $D_{LCP,f}$ stands for the fresh (without aging) LCP delay distribution. The path under analysis is assumed under maximum degradation conditions (See Section II) while the LCP is considered fresh, to assure that a discarded path does not become critical under any aging condition.

The threshold ε defines the acceptable degree of probability that a path under analysis becomes more critical than the LCP. The paths that exceed this threshold should be monitored. As ε value decreases, a higher number of critical paths are selected to be monitored, which means that circuit reliability increases. Using a small value of ε assures that a path not passing this criterion is quite unlikely to become critical in spite of process variations and aging conditions.

Criterion 2: Even if a path is selected with *Criterion 1*, it could exist another already selected path whose delays cover the delays of the path under analysis. Therefore, a second criterion is applied to the set of paths already selected with *Criterion 1*. This criterion establishes that a path does not need to be monitored if its probability of having delays greater than the delays of any other selected path with *Criterion 1* is lower than ε (See Equation 4).

$$P(D_{i,a} > D_{j,f}) < \varepsilon \tag{4}$$

Similar to *Criterion 1* the path i under analysis is assumed under maximum degradation conditions while the other path (j) is considered fresh.

*2) **Computing Selection Criteria**:* For two path delay distributions D_A and D_B, where D_A is for the LCP and D_B is for the path under analysis, *Criterion 1* can be translated to the probability that the *delay difference random variable* DD ($= D_B - D_A$) takes values greater than zero by the threshold value ε. This can be expressed as: $P(DD > 0) > \varepsilon$. *Criterion 1* is evaluated by obtaining the mean and variance of DD, which are given by equations 5a and 5b, respectively.

$$\mu_{DD} = \mu_{D_B} - \mu_{D_A} \tag{5a}$$

$$\sigma^2_{DD} = \sigma^2_{D_A} + \sigma^2_{D_B} - 2 \cdot COV(D_A, D_B) \tag{5b}$$

The mean (μ_{DD}) and the variance (σ^2_{DD}) of DD can be computed by means of SSTA. At early steps of the design flow, the mean value μ_{DD} can be estimated by a pre-characterization of nominal delays of the gates library. However, σ^2_{DD} estimation requires to compute the *paths variance* and the *inter-path covariance*, which depend on the spatial correlation between gates. Since actual layout gate placement information is not usually available at early design stages, an approach to estimate σ^2_{DD} without spatial correlation information will be presented in the next section.

Criterion 2 can be computed similarly to *Criterion 1*. In this case, DD is obtained between the path under analysis and each previously selected path with *Criterion 1*.

C. Nodes to be monitored

Only one single aging sensor per group of those selected paths converging at the same output node is required. This minimizes the total number of aging sensors that require to be placed at the output nodes.

Our cost−effective methodology allows the critical paths to be effectively covered by the inserted aging sensors and corrective actions can take place if a near-faulty behavior occurs in those paths.

IV. Early Selection of Critical Paths to be monitored due to NBTI aging

This section describes in detail our approach to evaluate the statistical selection criteria without spatial correlation information.

A. Computing the Delay Diference Probability Density Function

For two path delay distributions D_A and D_B, where D_A is for the reference path (i.e. the LCP) and D_B is for the path under analysis, the mean value of the delay difference probability density function μ_{DD} is given by Equation 6.

$$\mu_{DD} = \sum_{i \epsilon B}^{N} \mu_i - \sum_{i \epsilon A}^{M} \mu_i \tag{6}$$

where M and N are the number of gates in the paths A and B, and μ_i is the mean delay for gate *i*.

The variance of the delay difference distribution can be computed as shown in Equation 7.

$$\begin{aligned}\sigma^2_{DD} = &\sum_{i \epsilon A}^{M}\sum_{j \epsilon A}^{M} \rho_{ij} \cdot \sigma_i \cdot \sigma_j + \sum_{i \epsilon B}^{N}\sum_{j \epsilon B}^{N} \rho_{ij} \cdot \sigma_i \cdot \sigma_j \\ &- 2\sum_{i \epsilon B}^{N}\sum_{j \epsilon A}^{M} \rho_{ij} \cdot \sigma_i \cdot \sigma_j\end{aligned} \tag{7}$$

where ρ_{ij} is the spatial correlation between gates i and j, and σ_i and σ_j are the gate delay standard deviations for gates *i* and *j*, respectively. Note that each term of Equation 7 corresponds to one term in Equation 5b. Also note that ρ_{ij} in the first and the second sumation relates two gates in the same path while ρ_{ij} in the third sumation relates one gate in path A and one gate in path B.

Analytical models for spatial correlation can be found in literature, which considers it as an exponentially decreasing function of the distance between two gates [18]. However, placement information is not usually available at early design stages to compute spatial correlation.

B. Correlation Estimation at Early Design Stage

The values of spatial correlation required to compute the delay difference variance (See Equation 7) can be represented by a correlation matrix as in Equation 8. The term ρ_{ij} represents the spatial correlation between gates i and j. Matrix indexes highlighted in orange correspond to the spatial correlation between gates in the same path. Those values are used to compute each path variance (First two summations of Equation 7). Matrix indexes highlighted in blue corresponds to the spatial correlation between a gate in one path with a gate in the other path. Those values are used to compute the inter-path covariance (Third summation of Equation 7). It should be noted that if the gate i is the same gate j, the value of spatial correlation becomes the unit because it corresponds to the correlation of a gate with itself.

$$\rho_{ij} = \begin{pmatrix} \rho_{1_a1_a} & \rho_{1_a2_a} & \cdots & \rho_{1_aN_a} & \rho_{1_a1_b} & \rho_{1_a2_b} & \cdots & \rho_{1_aM_b} \\ \rho_{2_a1_a} & \rho_{2_a2_a} & \cdots & \rho_{2_aN_a} & \rho_{2_a1_b} & \rho_{2_a2_b} & \cdots & \rho_{2_aM_b} \\ \vdots & \vdots & \ddots & \vdots & \vdots & \vdots & \ddots & \vdots \\ \rho_{N_a1_a} & \rho_{N_a2_a} & \cdots & \rho_{N_aN_a} & \rho_{N_a1_b} & \rho_{N_a2_b} & \cdots & \rho_{N_aM_b} \\ \rho_{1_b1_a} & \rho_{1_b2_a} & \cdots & \rho_{1_bN_a} & \rho_{1_b1_b} & \rho_{1_b2_b} & \cdots & \rho_{1_bM_b} \\ \rho_{2_b1_a} & \rho_{2_b2_a} & \cdots & \rho_{2_bN_a} & \rho_{2_b1_b} & \rho_{2_b2_b} & \cdots & \rho_{2_bM_b} \\ \vdots & \vdots & \ddots & \vdots & \vdots & \vdots & \ddots & \vdots \\ \rho_{M_b1_a} & \rho_{M_b2_a} & \cdots & \rho_{M_bN_a} & \rho_{M_b1_b} & \rho_{M_b2_b} & \cdots & \rho_{M_bM_b} \end{pmatrix} \tag{8}$$

In order to evaluate the selection criteria under conservative assumptions due to spatial correlation uncertainty, σ^2_{DD} should be approximated in such way that its value is maximum, because it increases the probability that the Delay Difference Distribution takes values greater than zero.

The approximation of σ^2_{DD} can be made assuming spatial correlation bounds. For example, the spatial correlation to compute each path variance becomes the unit (gates are assumed fully correlated), while the spatial correlation to compute covariance between paths becomes zero (gates are assumed completely uncorrelated) [13]. However, this first approach would result in a significant overestimation of the number of paths to be monitored. Figure 4 plots the terms of Equation 5b obtained for each pre-filtered path (B_i) and the LCP (A) of ISCAS $C1908$ circuit. Each dot represents a different path in the circuit. The data for this figure has been obtained directly using spatial correlation information from layout. Figure 4 shows that there is a behavior relationship between the sum of the first two terms of Equation 5b and the third term. This trend was also observed for other ISCAS benchmark circuits. Hence, previous spatial correlation bounding approach would result in a significant overestimation of the critical paths set to be monitored. Based on this observation, a first approximation is made:

Approximation 1*: A same correlation value to compute each path variance and inter−path covariance is assumed.*

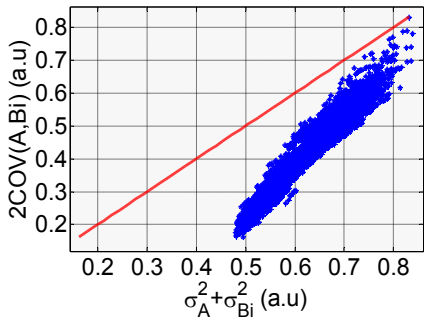

Figure 4. Behavior between addition of paths delay variances and their covariance computed for the LCP and each analyzed path of C1908 circuit.

This means that all the elements in matrix 8 that are not the unit are replaced by the global correlation ρ_g. This assumption introduces a trade-off between the added terms (path

variances) and the substracted term (inter-path covariance) because both increase as ρ_g increases.

A second issue is to determine the ρ_g value that should be used to maximize σ^2_{DD} under these global correlation assumption. Figure 5 shows two inverter chains that were analyzed to solve this issue. The path in the top is assumed the LCP with $M = 20$ inverters, and the path in the bottom is the path under analysis with N stages going from 2 to 20 inverters. σ_{DD} was computed for different ρ_g values as shown in Figure 6. It can be observed that for a short path ($N << M$), σ_{DD} is maximized by $\rho_g = 1$. However, for a long path ($N \approx M$), $\rho_g = 0$ provides an upper bound for σ^2_{DD}. In general, it would be expected that logic depths of the critical paths, including the LCP, are not dramatically different from each other. Similar results have been found for others types of gates structure, such as $NANDs$ and $NORs$. Based on this observation, a second approximation is made:

***Approximation 2**: A value of $\rho_g = 0$ is used.*

Some logic paths could miss the previous maximization property, but if this set is reduced it would not significantly impact our proposed approach. It must be noted that an exception of *Approximation* 2 are those gates with structural correlation where $\rho_g = 1$ is used.

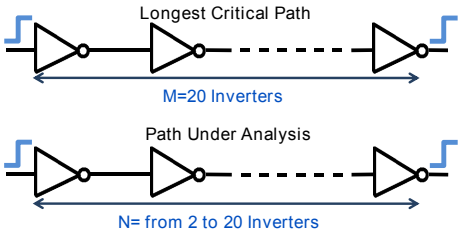

Figure 5. Inverter chains to analyze the impact of ρ_g on the standard deviation of the delay difference (σ_{DD}) as function of the path depth.

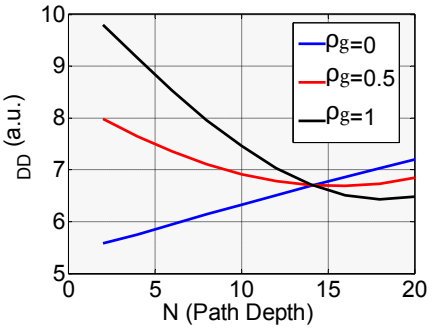

Figure 6. Impact of ρ_g on σ_{DD} as function of the depth of the path under analysis.

V. Simulation Results

The proposed methodology has been applied to some ISCAS85 benchmark circuits implemented in a commercial $65nm$ technology. Mentor Graphics suite of layout, synthesis, simulation, and DFT tools were used. Table I shows main characteristics of the analyzed circuits. It can be seen that the number of pre-filtered paths do not significantly decrease with respect to the number of topological paths. This is because corned-based static timing analysis with conservative aging gives a very pessimistic selection of critical paths.

Table I
Circuits Characteristics of the ISCAS85 Benchmark Circuits

Circuit	Gates Number	Topological Paths	Output Nodes	Pre-filtered Paths
C432	168	82364	7	81884
C499	220	9440	32	9408
C880	226	4935	26	4566
C1908	244	15638	25	15330
C2670	393	3381	50	1896
C3540	748	670373	22	659495
C5315	1139	24662	123	23112
C7552	1365	43614	108	40512

The results obtained with our proposed early design methodology for different probability thresholds ε are shown in Table II. The number of selected critical paths and the number of nodes to be monitored are given. The set of paths to be monitored selected statistically (See Table II) is significantly smaller than the set of pre-filtered paths (See Table I). A high number of critical paths can be covered by monitoring few output nodes (See Table II). The results are given for three ε values, which set the degree of circuit reliability as defined in Section 4b (See equations 3 and 4). Circuit reliability increases as lower values of ε are used. This is because a more stringent selection criterion allows to select more critical paths. It can also be observed that the number of nodes to be monitored remain the same as ε reduces from 1% to 0.5% in spite that more critical paths were selected. This is because the additional selected critical paths converge at the already selected output nodes with ε=1%. However, the number of output nodes increase in ISCAS $C7552$ for ε=0.25% (from 12 to 13). An aging sensor also must be inserted at the new output node to cover new selected critical paths do not covered previously by ε values of 1% and 0.5%.

Table II
Results with our proposed early methodology.

Circuit	$\varepsilon = 1\%$		$\varepsilon = 0.5\%$		$\varepsilon = 0.25\%$	
	Selected Paths	Nodes to Monitor	Selected Paths	Nodes to Monitor	Selected Paths	Nodes to Monitor
C432	4720	3	5298	3	5883	3
C499	2304	32	2384	32	2432	32
C880	80	3	86	3	93	3
C1908	283	7	333	7	370	7
C2670	84	1	92	1	100	1
C3540	1052	3	1174	3	1280	3
C5315	166	4	184	4	200	4
C7552	95	12	114	12	126	13

In order to validate our proposal, the results obtained with the proposed methodology have been compared against those obtained using SSTA with layout information [9]. The analytical model proposed in [18] was used to calculate the

Table III
RESULTS USING LAYOUT INFORMATION.

Circuit	$\varepsilon = 1\%$		$\varepsilon = 0.5\%$		$\varepsilon = 0.25\%$	
	Selected Paths	Nodes to Monitor	Selected Paths	Nodes to Monitor	Selected Paths	Nodes to Monitor
C432	4676	3	5248	3	5816	3
C499	2272	32	2315	32	2400	32
C880	78	3	82	3	92	3
C1908	270	7	317	7	347	7
C2670	81	1	89	1	95	1
C3540	1030	3	1153	3	1242	3
C5315	186	4	209	4	220	4
C7552	95	12	116	13	126	13

spatial correlation. Table III shows the number of selected critical paths and nodes to be monitored obtained from layout-based analysis. The comparison of the proposed methodology result (See Table II) against the layout-based results (See Table III) makes evident that our approach approximates quite well the number of critical paths and nodes to be monitored. Differences between the selected paths in Table II with those selected in Table III may contain some wrong selected paths (paths considered as critical but actually they are not) and some unselected paths (paths not identified as critical but that actually they are). However, the fact that many paths could converge at the same output node makes that even if a path is not actually selected by the proposed methodology, it is still covered if it shares its output node with at least one selected path. As can be seen, for almost all cases, the correct number of nodes to be monitored was identified. Only for $C7552$ with $\varepsilon = 0.5\%$, an output node is not selected with the early design methodology. However, using in the early methodology an ε value lower than that used in the layout-based analysis makes less likely that a true critical path is unselected. Thus, some nodes and paths do not selected can be included in the predicted critical path set (compare columns 4 and 5 from Table III with columns 6 and 7 from Table II).

VI. CONCLUSIONS

An early prediction methodology for aging sensors insertion in an error prediction framework has been proposed. The combined effect of process variations and aging due to NBTI were taken into account. To approximate the locations where aging sensors should be inserted, paths that are likely to become critical are identified first. Two statistical criteria are used to select the critical paths set to be monitored. The set size depends on the desired degree of circuit reliability.

The proposed methodology is suitable to be applied at an early design step, which reduce design complexity since computation of spatial correlation between each pair of gates in the circuit is not required. To handle the lack of spatial correlation information a statistical non-layout dependent approach that maximizes the probability of a critical path to be identified was proposed. A comparison of the proposed methodology with that based in availability of layout information shows that our proposal accurately predicts the set of critical paths and nodes to be monitored.

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