Analysis of FPGA SEU Sensitivity to Combined Effects of Conducted EMI and TID

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***Abstract*— This work proposes a novel methodology to evaluate SRAM-Based FPGA SEU susceptibility to noise on V_{DD} power pins and total-ionizing dose (TID). The procedure was demonstrated for SEU measurements on a Xilinx Spartan 3E FPGA operating in an 8MV Pelletron accelerator, whereas TID was deposited by means of a Shimadzu XRD-7000 X-ray diffractometer. The injected noise on power supply bus comprised of voltage dips of 16.67% and 25% of V_{DD} at two different frequencies 10Hz and 5kHz, and was performed according to the IEC 61.000-4-29 international standard.**

***Index Terms*—SEU Sensitivity, SRAM-Based FPGA, Power-Supply Noise, EMI, TID, Combined Test, Spartan 3E.**

I. Introduction

The widespread use of Field-Programmable Gate Arrays (FPGAs) in our daily lives has become a general consensus among IC and embedded system designers, with numerous applications in the fields such as telecommunication, automotive [1], medical and aerospace & defense [2]. However, the latter application field requires not necessarily competitive costs but instead, highly reliable devices by default. In this sense, SRAM-based FPGAs are pretermitted with respect to flash or anti-fuse devices [3]. This is the case of FPGAs used in the design of embedded systems for satellite applications due to the continuous sensitivity increase to single-event upset (SEU), electromagnetic interference (EMI) and total-ionizing radiation (TID) [4,5]. This is particularly true for SEU and EMI because IC sensitivity deteriorates as technology scales down. Note that for smaller geometry technologies, information is stored in smaller capacitors, clock frequency tends to increase and power supply is driven to values much lower than 1 volt, which renders ICs more sensitive to noise and external perturbations such as SEU and EMI.

Furthermore, the process of qualifying ICs to critical applications is usually treated as an independent, fragmented event, i.e., engineers certify devices to EMI, TID or SEU or eventually to all of them, but often not taking into account the combined effects one phenomenon may take over the other. In this scenario, this paper proposes a novel methodology to analyze the SEU sensitivity of FPGA devices to combined effects of conducted EMI and TID. The procedure was demonstrated for SEU measurements on a Xilinx Spartan 3E FPGA exposed to combined noise on power supply bus comprised of voltage dips of 16.67% and 25% of V_{DD} at frequencies of 10Hz and 5kHz respectively, and total-ionizing dose (TID). Noise was injected according to the IEC 61.000-4-29 standard [6].

II. Methodology Description

Hereafter, the methodology is introduced by describing an experiment performed on two Xilinx/Spartan 3E FPGAs (part number XC3S500E-4PQ208), from different fabrication lots. In the remaining of the paper, these devices under test (DUTs) are identified as FPGA1 and FPGA2. The test flow applied to these components is depicted in Fig. 1. Both FPGAs were sitting on a new version of a dedicated, configurable platform for IC combined tests of total-ionizing dose radiation and electromagnetic interference, whose first version was introduced in [7]. Initially, a functional test was performed to check the fresh component nominal operating conditions: minimum operating voltage (V_{DDmin}) and average dynamic current (I_{DDave}).

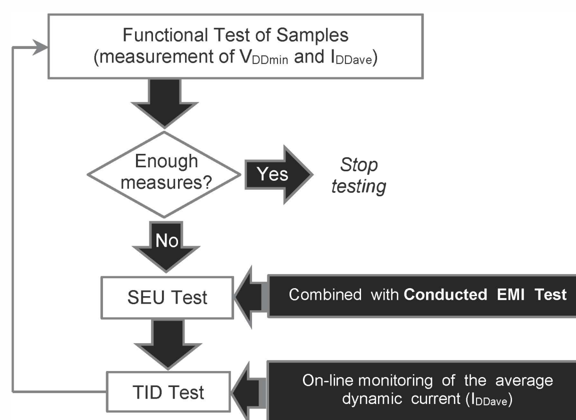

Fig. 1. Test flow applied to the two Xilinx Spartan 3E FPGAs.

For the functional test and the TID test, the DUTs were configured with the LEON3 softcore processor [8] running a bubble sort program. LEON3 is a synthesizable VHDL model of a 32-bit 7-stage pipeline processor compliant with the SPARC V8 architecture. The model is highly configurable, and particularly suitable for system-on-a-chip (SoC) designs.

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The full source code is available under the GNU GPL license, allowing free and unlimited use for research and education. LEON3 is also available under a low-cost commercial license, allowing it to be used in any commercial application to a fraction of the cost of comparable IP cores. The ISE-Xilinx design framework was used to configure and validate the embedded system (i.e., the processor and the bubble sort program) on the fresh Spartan 3E FPGAs.

Then, the SEU test was initiated in order to measure the SEU susceptibility of the two DUTs by exposing them to heavy ions inside an 8MV Pelletron accelerator (see Fig. 2a). The devices were irradiated with the following ions: ^{12}C, ^{16}O, ^{28}Si and ^{35}Cl.

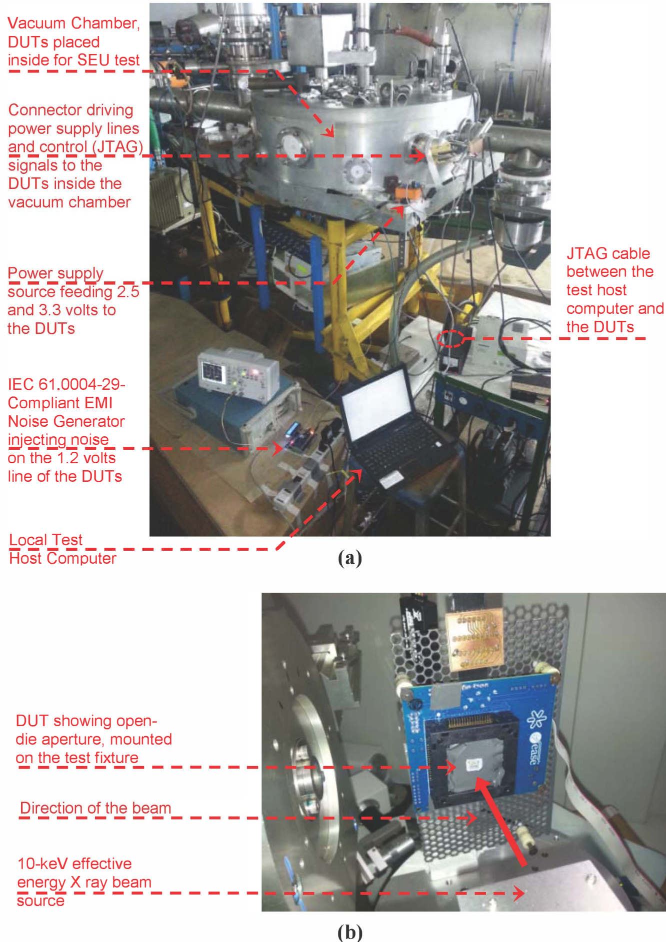

Fig. 2. Test environment: **(a)** 8MV Pelletron accelerator, **(b)** 10-keV Shimadzu XRD-7000 X-ray diffractometer.

In the sequence, the TID test was initiated by exposing the DUTs to a 10-keV effective energy X ray beam in a Shimadzu XRD-7000 X-ray diffractometer (see Fig. 2b). It was used 100 rad/s dose rate during this process. The irradiation period was controlled in order that the total doses absorbed by the devices were 750 krad and 950 krad. The samples were held 10 cm away from the beam source to ensure homogeneity in the area to be irradiated. The dose rate was estimated by measuring exposure in an ionization chamber and the X-ray dose rate in silicon was calibrated using air and silicon mass attenuation coefficients. The effective energy was measured using aluminum foils of different thickness and calculating the half–attenuation Al layer. In fact, for TID effects, 10 keV X-ray radiation is a very convenient source of radiation owing to its higher charge yield compared to protons, alpha particle and heavy ions. The above test flow was repeated twice for each of the FPGAs: in the first run, it was deposited 150 krad on FPGA1 and 400 krad on FPGA2, whereas in the second run it was deposited additional 600 krad on FPGA1 and 550 krad on FPGA2. At the end of the experiment, these devices received a total ionizing dose of 750 krad (FPGA1) and 950 krad (FPGA2).

III. Obtained Results and Discussions

Fig. 3 presents the FPGA1 SEU cross section as a function of **(a)** voltage reduction: from the nominal value (1.2 volts) down to 800 mV; and **(b)** noise on power supply lines (16.67% voltage dips on V_{DD}, at a frequency of 10 Hz). The bit-flip counting procedure was conducted by performing continuous readback of the configuration bitstream of the FPGA. It is worth mentioning that in this case, the configuration bitstream was composed of the configuration bits plus the BlockRAM bits used to store user information. As observed, when V_{DD} is reduced from 1.2 to 0.8 volts (33.33%), the average FPGA1 SEU sensitivity (configuration bits + BlockRAM bits) increases from 3.16 x 10^{-9} cm^2/bit to 3.53x10^{-9} cm^2/bit (i.e., 11.70%). For those readers not familiar with SEU practical experiments, it is worth noting the definition of *SEU cross section* as being *the total area of the circuit such that, if exposed to radiation, there will be SEUs*. So, as larger is the SEU cross section, more sensitive is the circuit to single-event upsets.

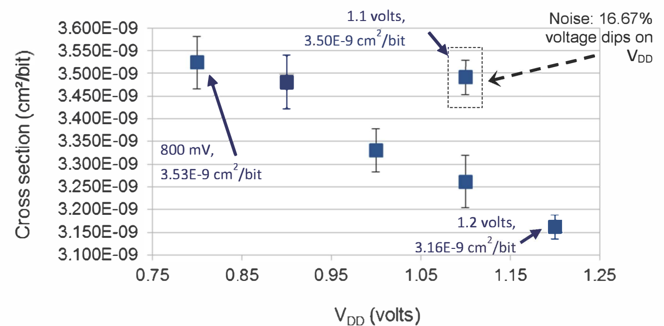

Fig. 3. FPGA1 SEU cross section as a function of: **(a)** voltage reduction from the nominal value (1.2 volts) down to 800 mV; and **(b)** noise on power supply lines (16.67% voltage dips on V_{DD}, at a frequency of 10 Hz). Results for fresh component.

It is important to note that noise on power supply lines seems to be more harmful to the FPGA SEU sensitivity than V_{DD} reduction: SEU cross section increases from 3.16 x 10^{-9} cm^2/bit to 3.50x10^{-9} cm^2/bit (i.e., by 10.76%) when 16.67% voltage dips are applied on V_{DD}, which is quite close to the 11.70% SEU cross section degradation (3.53x10^{-9} cm^2/bit) for a V_{DD} = 800 mV (33.33% voltage reduction on V_{DD} bus). In other words, **16.67% voltage dips on V_{DD}** induces the same SEU cross section as the one yielded by **reducing V_{DD} by 33.33%**. From this scenario and aiming to guarantee a given SEU cross section, one could suggest design engineers to take

more care to prevent noise than small power supply reductions from appearing on the FPGA bus during system lifetime. This goal can be reached, for instance, by implementing specific RC filters at the FPGA input power pins so that to prevent external noise from entering the chip [9]. The same experiment was also carried out with FPGA2, which yielded similar results. In this case, it was applied 5 kHz, 25% voltage dips on the V_{DD} bus.

Fig. 4 provides results for FPGA1 at three different instants: fresh, after deposition of 150 and 750 krad. As observed, as long as radiation is being deposited, SEU cross section is being increased by a factor of 5.16% with respect to the fresh condition (averaged 5 measurement points for 150 krad curve divided by the averaged 5 measurement points of the fresh curve) and 7.55% (resp. 750 krad curve). At the same time, one can also conclude that no matter the component is fresh or irradiated, SEU cross section increases dramatically as response to V_{DD} reduction from 1.2 to 0.8 volts: SEU cross section degrades in average 11.40% for fresh device, 6.57% for the 150 krad irradiated device and 7.85% for the device with 750 krad.

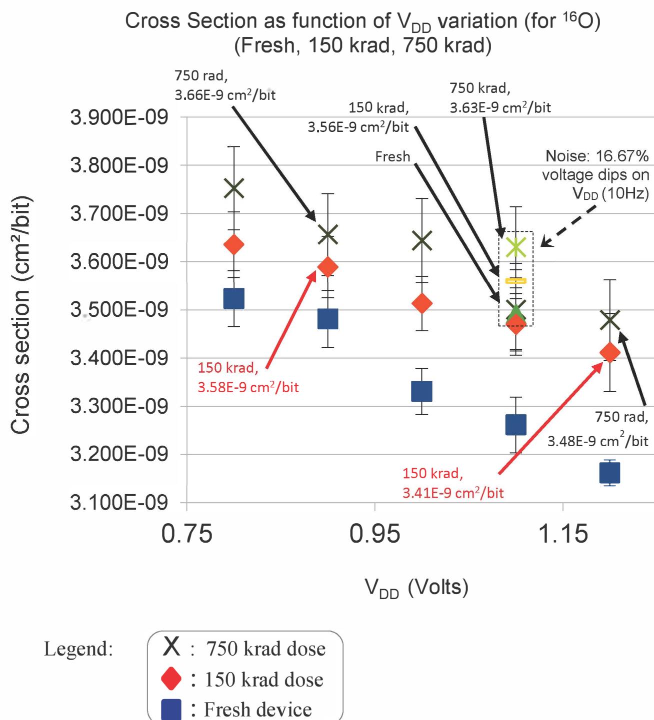

Fig. 4. FPGA1 SEU cross section as a function of: **(a)** voltage reduction from the nominal value (1.2 volts) down to 800 mV; and **(b)** noise on power supply lines (16.67% voltage dips on V_{DD}, at a frequency of 10 Hz). Results for fresh, 150 and 750 krad component.

Finally, the combination of "noise on power pins plus TID" is more harmful to the chip than the combination of "V_{DD} reduction + TID", as can be observed: for the fresh component, 16.67% voltage dips on V_{DD} induces similar SEU cross section as the one yielded by reducing V_{DD} by 33.33%. This behavior can also be observed for the irradiated component:

A) 16.67% voltage dips on V_{DD} induces a SEU cross section increase (at 3.56×10^{-9} cm²/bit, **150 krad curve**, with respect to 3.41×10^{-9} cm²/bit, V_{DD} = 1.2 volts), quite similar to the SEU cross section (3.58×10^{-9} cm²/bit, V_{DD} = 0.9 volts) induced by **25% V_{DD} reduction**.

B) 16.67% voltage dips on V_{DD} induces a SEU cross section increase (at 3.63×10^{-9} cm²/bit, **750 krad curve**, with respect to 3.48×10^{-9} cm²/bit, V_{DD} = 1.2 volts), quite similar to the SEU cross section (3.66×10^{-9} cm²/bit, V_{DD} = 0.9 volts) induced by **25% V_{DD} reduction**.

IV. CONCLUSIONS

This paper briefly described a dedicated methodology to analyze the SEU sensitivity of FPGA devices to combined effects of conducted EMI and TID. The procedure was demonstrated for SEU measurements on a Xilinx Spartan 3E FPGA device (part number XC3S500E-4PQ208). The injected noise on power supply bus comprised of voltage dips of 16.67% and 25% of V_{DD} at frequencies of 10Hz and 5kHz respectively, and it was performed according to the IEC 61.000-4-29 international standard.

Analyzing Fig. 4, one can conclude that noise (16.67% voltage dips on V_{DD}, 10Hz) induces similar SEU cross section as the one yielded by reducing V_{DD} (33.33%). So, at least for this frequency and for this component, noise on power bus pins seems to be more harmful to SEU cross section than V_{DD} reductions.

At present, we are analyzing and comparing the impact of low-frequency and high-frequency noises on the SEU cross section degradation of FPGA2 (which received a total ionizing radiation of 950 krad and operated under exposition of 25% voltage dips at frequency of 5 kHz . Preliminary experiments indicate that low-frequency noise induces more SEU cross section degradation than the high-frequency one. This conclusion will be confirmed by means of future experiments to be conducted with the same components, for similar voltage dips and frequencies in the range of [10 - 5kHz] and above. Currently, we are also repeating similar experiments with the flash-based ProASIC3 A3PE1500 FPGA from Microsemi.

ACKNOWLEDGEMENTS

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