An LSSD Compliant Scan Cell for Flip-Flops

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***Abstract*—Most recent timing resilient templates are using asynchronous design techniques and integrating both flip-flops and latches in their design to enable more aggressive performance improvement and reduction in energy consumption. Despite these benefits, they impose challenges in terms of testability because both latches and flip-flops typically use different test protocols. This paper presents an optimized scan cell for flip-flops which is compatible with the protocol used by scannable latches. By using the proposed cell, it is possible to have latches and flip-flops in the same scan chain and the DfT flow fully automated by commercial EDA tools. Experimental results show that the proposed cell reduces silicon area, leakage, and dynamic power compared to the original cell.**

***Index Terms*—VLSI testing, flip-flop scan cell, level sensitive scan-based design (LSSD).**

I. Introduction

The quest for high performance circuits with low power consumption under a technology node prone to high variability is pushing VLSI design approaches towards different circuit techniques such as timing resilient circuits. These techniques allow removing or reducing timing margins included in the design to cope with variability, increasing circuit performance. Furthermore, they can also reduce the circuit voltage up to an acceptable level of violations to reduce the power consumption. The timing resilient circuits templates have an Error Detection Logic (EDL) responsible for detecting timing violations in the critical path, and for triggering a corrective action to recover from the error before a system failure occurs. There are several types of recovery actions such as inserting bubbles into the pipeline, flushing the pipeline or delaying a handshake protocol.

The timing resilient templates can be synchronous, as in [1]–[3], or asynchronous, as in [4], [5]. Asynchronous resilient templates combine the advantages of resilient circuits and asynchronous design style to allow more aggressive performance improvements and power reductions [6]. The resilient templates can also be classified in terms of the base memory element used in their sequential logic blocks, which are either based only on flip-flops [3], or on both latches and flip-flops [1], [4], [5]. Although there are several proposals of resilient templates, the same cannot be said about the proposals to test circuitry for resilient circuits. For instance, detecting manufacturing faults in the EDL is of uttermost importance because it has been demonstrated that a single stuck-at fault in the EDL is enough to disable its ability to detect and recover from timing violations [7]. Moreover, most of the resilient templates rely on increasing the memory cells of the circuit by adding the so called shadow latch. This implies an extra area to implement the DfT strategy on top of the additional area to implement the resilient circuit itself [8], [9]. As mentioned before, some of the most recent approaches for resilient templates are based on bundle data asynchronous design that use both D latches and flip-flops [4], [5]. This places additional challenges to its DfT strategy regarding the preferable scan protocol to be used.

The first approach to address this issue is, for example, to build different scan chains, one for the flip-flops using D-Mux scan cells [10] and the other scan chain consisting only of latches, based on Level-Sensitive Scan Design (LSSD) scan protocol [11]. However, commercial DfT EDA tools do not allow both test protocol in the same design, so only one protocol must be chosen. The second approach, targeted by this paper, *is to use a scannable flip-flop compatible with the LSSD test protocol*. This enables combining both the scannable latches and flip-flops in the same LSSD-based scan chain. However, this cell is not readily available in most technology libraries. Thus, the *goal of this paper is to present an open cell design of an optimized scannable flip-flop compatible with the LSSD test protocol, called Clocked-LSSD, along with a methodology to design this cell in a target technology and integrate it in conventional EDA flows*.

II. Motivation

Contemporary design styles for synchronous and asynchronous integrated circuits rely on the usage of both latches and flip-flops and thus require specific techniques for DfT. This Section presents examples of circuits that motivated the proposal of the Clocked-LSSD cell.

A. Razor Template

The Razor template is a synchronous architecture [1] that allows eliminating worst-case safety margins in the clock period by using a novel voltage management technique, where the processor operates with dynamic voltage scaling (DVS). This technique replaces the flip-flops on critical paths of the design by Razor Flip-flops. The clock signal controls the Main Flip-flop and the Shadow Latch is controlled by a delayed clock. To detect a timing violation, the Razor Flip-flop compares the values stored in the Main Flip-flop and in the Shadow Latch. If the values are different, then an error is detected. A set of simulated benchmark experiments shows

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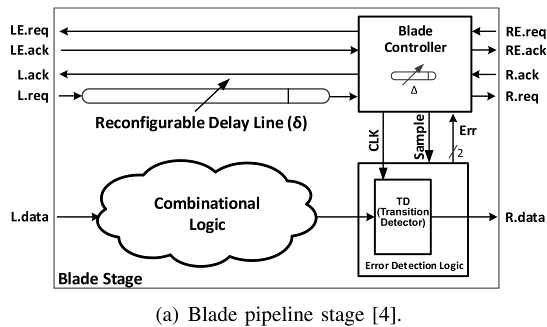
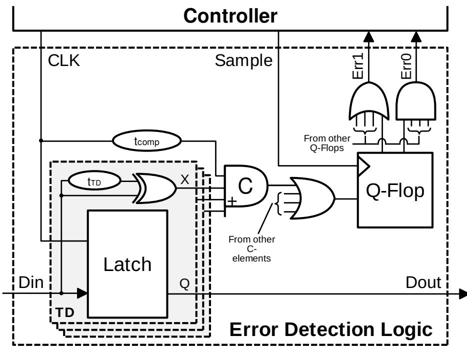


(a) Blade pipeline stage [4].



(b) Blade's Error Detection Logic [4].

Fig. 1: Blade timing resilient template.

that an error rate of 1.5% allows an average energy savings of 41% with a maximum performance slowdown of 6%.

B. Blade Template

Blade [4] is a metastability-free asynchronous template for 2-phase bundled-data (BD) circuits. Figure 1(a) illustrates the basic Blade architecture, represent by a pipeline stage. It consists of a controller, two configurable delay lines (δ and Δ), and an error detection logic (EDL). The controller uses a BD channel **L/R** to communicate with others pipeline stages. The delay δ is used to control the moment that data can be sampled and propagated through the EDL. The delay Δ is used to define the amount of time the latch is transparent and the timing resilience window (TRW), which is a period where errors can be detected and recovered. The signal **Err** is a dual-rail signal used to flag a timing violation to the controller.

Figure 1(b) details the EDL. The design consists of a latch-based transition detectors (TD) used to capture setup violations, asymmetric C-elements and Q-Flops [12] used to store any violation detected. The Q-Flop consists of a flip-flop and a metastability filter which guarantees metastability-free signals to the Blade controller. The Blade controller is implemented using Burst-mode state machines, but can also be implemented using the Click template [13]. A 3-stage version of the Plasma microprocessor[1] (based o MIPS-I instruction set) targeting a 28nm FD-SOI technology was used as a case study, presenting 8.4% of silicon area overhead and 19% of performance improvement when compared to the original synchronous design.

[1]https://opencores.org/project,plasma

C. Sharp Template

Sharp [5] is another asynchronous resilient template derived from Blade. It consists of one handshake channel on each side of the controller, and each channel is composed of tree signals: **Open**, **Close** and **Acknowledge**. The **Open** and **Close** signals also control the TRW in the Sharp controller. Sharp has two delays: θ and λ. θ is important to ensure the correctness of the circuit. λ is used in the speculative handshake protocol implemented by this template. Like Blade, Sharp also uses an EDL to capture setup violations. The results show that Sharp achieves 8% higher throughput than Blade.

D. Discussion

Literature shows that modern pipelined circuits can rely on both latches and flip-flops as sequential elements, in either synchronous or asynchronous design styles. For example, the Razor template uses latches to help detecting timing errors, and Blade and Sharp use latches in the data path and can use flip-flops in the controllers. Accordingly, the Q-Flop cell in Blade's EDL is built on top of a Flip-flop cell. As far as we could verify, no work available in the state-of-the-art explores on how to test these circuits using predefined standards compatible with conventional tools. In fact, the only work that explores specific testability issues of mixing latches and flip-flops in these architectures is [8]. Yet, their proposal is an ad-hoc solution with specific circuitry that requires a manual definition of test structures. Therefore, a methodology to allow automated insertion of DfT infrastructure and ATPG is required.

III. State-of-the-Art on Testable Latches

This Section shows existing solutions to build scan chains on circuits that mix latches and flip-flops as memory elements.

A. Clocked-LSSD

Eichelberger and Williams [11] proposed a way to test latch-based designs called Level Sensitive Scan-based Design (LSSD) test protocol. However, when a design mixes latches and flip-flops, it is necessary to have an LSSD compliant scan cell to replace both types of cells. An LSSD compliant cell for latch and for flip-flop are illustrated, respectively, in Figure 2 and Figure 3(a). The "*" in Figure 2 divides the functional input pins (**C** and **D**) and the test input pins (**A**, **B** and **I**).

The LSSD single-latch cell in normal mode has a D latch behavior, which means that the memory elements are level sensitive. In test mode, the operations are performed using the test clocks. The Clocked-LSSD has a D flip-flop behavior in normal mode, which means that the memory elements are edge-triggered. In test mode, the Clocked-LSSD has the standard LSSD behavior mentioned before, which means that the memory elements are level sensitive. Figure 3(b) shows the Clocked-LSSD truth table. The "R" means that the system data is registered at clock rising edge and the "*" at the clocks **A** and **B** means that clock **A** must pulse before clock **B**. However, this original cell has a big area overhead because it is composed by tree latches, while a standard flip-flop has two latches.

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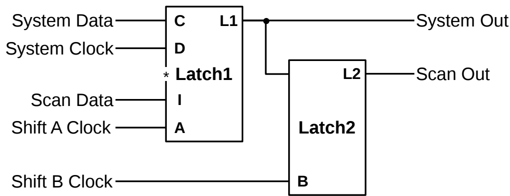
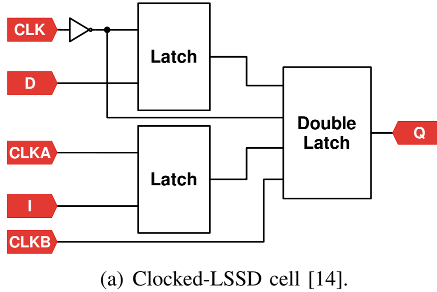


Fig. 2: LSSD single-latch register level [12].



(a) Clocked-LSSD cell [14].

	D	CLK	I	CLKA	CLKB	Q
Normal Mode	0	R	x	0	0	0
Normal Mode	1	R	x	0	0	1
Normal Mode	x	x	0	0	0	Q
Test Mode	x	0	0	1*	1*	0
Test Mode	x	0	1	1*	1*	1

(b) Clocked-LSSD truth table [14].

Fig. 3: Clocked-LSSD behavior.

B. Patented Design

There is a reduced set of works about Clocked-LSSD in contemporary literature. Yurash [15] patented an optimization of Clocked-LSSD that uses two latches instead of tree latches in the original design. This cell has 40 transistors against 48 transistors required by the original cell design. However, this patent presents a different test protocol that is not compliant with the standard defined for Clocked-LSSD, see Figure 3(b).

Unlike the conventional Clocked-LSSD, this cell requires that the system clock is kept at a high logic value during the shift operation, as showed in Figure 4. In the original test protocol, the system clock is at 0 logic value during this operation. If the clock is at low logic value during the shift operation in the patent cell, the data at input **SI** does not pass through the first latch, interrupting the operation. Moreover, this cell needs an overlap between the clocks **A** and **B** (as showed in Figure 4), while in the LSSD test protocol does not allow the test clock overlap to avoid a race condition. Thus, this implementation is not directly compatible with contemporary standards and commercial synthesis tools, significantly reducing the levels of automation provided for designs using it.

IV. LSSD Compliant Scan Cell for Flip-Flops

A. Proposed Optimization

This Section describes the proposed optimization of the conventional Clocked-LSSD. Figure 5 shows the schematic of the proposed optimized cell. As the cell proposed by

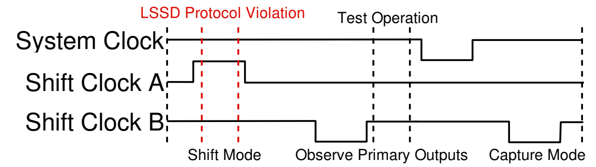


Fig. 4: LSSD protocol violation in Yurash's [15] cell.

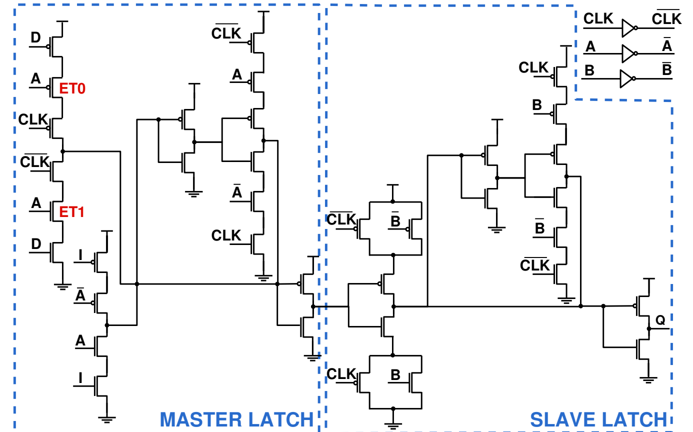


Fig. 5: Optimized Clocked-LSSD schematic.

Yurash, this optimization uses two latches, but has 2 additional transistors (**ET0** and **ET1**). These 2 transistors ensure that the proposed optimization cell has the same test protocol presented in Figure 3(b).

The sizing of transistors that generate the output **Q** must be according to the driving strength of the cell, as they are responsible for driving an output load. The input transistors must be sized to be used as an amplifier, recovering the input signal in case of loss caused by noise. Furhtermore, transistors of the feedback loops are minimum sized because they are only used for storing values, and not to drive output loads. Because the implementation relies in a static cell topology, such option for the feedback loop does not jeopardize reliability. Note that, if semi-static approaches are used, detailed noise analysis are required.

Note that although it may look like making Yurash's cell compliant to current standards and compatible with tools is just a matter of inverting the system clock signal, the truth is that a review in this cell is needed to ensure the correct test protocol behavior. The clock inversion just changes the clock edge, and the test protocol violation still happens once the clock must be active during the test operation. In the proposed optimized cell, it is necessary only these extra transistors to implement the logic that ensure the non-influence of data **D** selector in the behavior of the cell when the clock **A** is at logic level 1. Thus, this cell can be integrated with the commercial synthesis tools.

B. Results and Discussion

This Section compares the conventional Clocked-LSSD and the proposed cell. Note that, because the Yurash's cell is not compatible with the protocol used by the synthesis tool, is not possible to perform a comparison between this cell and

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TABLE I: Area and power evaluation of the synchronous XTEA with full scan.

	Area (μm^2)	Leakage Power (nW)	Dynamic Power (nW)	Fault Coverage For Stuck-At (%)
With Dft Using the Conventional Clocked-LSSD	1,061,34.35	1,275,976.24	4,742,273.18	100.00
With Dft Using the Proposed Clocked-LSSD	88,203.24	985,096.69	1,815,258.32	100.00
Optimized Clocked-LSSD reduction (%)	16.89	22.79	61.72	-

the proposed optimized cell using standard EDA tools. The results are limited to the logic synthesis level. Both cells were designed targeting the $28\,\mathrm{nm}$ FD-SOI technology and logic synthesis is performed using these cells and the core library provided by the technology vendor. Note that the designed cells do not have a layout implementation. Thus, cell area is estimated based on the size of cells present in the core library with similar transistor count and topology. In this specific case, traditional latch cells were used as a basis for the estimations, given their transistor topology. The proposed cell, showed in Figure 5, has an estimated area of $6.8\,\mu m^2$, while the conventional cell has an area of $7.8\,\mu m^2$.

A *synchronous version* of a pipelined XTEA criptocore [16] was chosen as the case study to perform the synthesis and DfT insertion using both Clocked-LSSD cells. The reason behind the choice for this design is that it enables a controlled environment for inserting test cells and comparing results, as it is a simple pipeline with well defined sequential stages and combinatorial logic. Accordingly, the XTEA design has data inputs of 64 bit width, a 128 bits key input and a 64 bits data outputs. This design has 32 pipeline stages, 23,734 combinational cells, and 6,238 D flip-flop cells. The circuit is synthesized targeting a 200MHz frequency.

Synopsys Design Compiler and DFT Compiler are used to perform logical synthesis and automatic *full scan* insertion. Two designs are generated, one using the conventional Clocked-LSSD and one using our proposed cell. To perform the power analyses, a value change dump (VCD) is generated by a simulation with delay provided by the standard delay format (SDF) generated in the logic synthesis. Table I shows the test overhead reduction of the proposed optimized cell.

After scan insertion, both XTEA designs obtained 100% of fault coverage for stuck-at faults with the Synopsys' Tetra-MAX ATPG tool. As the table shows, the circuit that used the proposed Clocked-LSSD presents an area reduction of 16.89% when compared with the circuit using the conventional Clocked-LSSD. Also, this reduction was of 22.79% and 61.72%, respectively, considering leakage and dynamic power data. The leakage reduces due to the number of transistor reduction in the proposed optimized cell, once the leakage power has relation with the number of transistors. The dynamic power has a significant reduction due to the extras transistors **EXT0** and **EXT1**, once they prevent the master latch data selection to active simultaneously and not propagating the switching through the circuit. The transistor configuration of the slave latch also contributed to this reduction, once the master latch of the conventional Clocked-LSSD is implemented using a double latch, and the optimized version is implemented with a single latch.

The second experiment uses a *Blade version of an equivalent XTEA design*. This design has 15,644 latches (where 4,794 of these latches were protected by Blade's EDL) and 401 flip-flops used to implement Q-Flops of Blade template. Thus, only 2.49% of the design's total number of memory elements corresponding to flip-flops. All the latches were automatically replaced by the LSSD cell. All the flip-flops were automatically replaced by the proposed cell, to allow exposing its impact in the circuit. The total area of XTEA with Blade (without scan chain) is $64,695.58\ \mu m^2$, while the version with DfT has $137,260.11\ \mu m^2$, generating an overhead of 112.16%. Most of this overhead is caused by the LSSD cell, which presents a high area increase ($6.2\ \mu m^2$) when compared with the standard latch cell ($1.47\ \mu m^2$). 1.98% of the total area corresponds to the Clocked-LSSD cell. Interestingly though, as observed in [4], the Blade template allows trading off resilience and silicon area overhead, which means that the designer can choose how many critical paths become timing resilient. It also means that the reported silicon area with the proposed cell can change accordingly, allowing large design space exploration for DfT insertion.

V. Conclusion

This paper presents an optimized version of the Clocked-LSSD scan cell that can be used to create scan chains of designs based on both latches and flip-flops as memory elements. The existing flip-flops of a design can be replaced by the proposed scan cell, compatible with the level-sensitive scan-based test protocol. This optimized cell is compatible with commercial DfT insertion and ATPG tools, allowing an automated DfT flow. A crypto core designed with two different design approaches, one synchronous design and other an asynchronous design, is used to demonstrate that the proposed cell presents lower silicon area and power when compared with the conventional Clocked-LSSD. Future work includes a characterization of the cell performance, a comprehensive analysis on the impact of process variability in the performance and reliability of the proposed design, and the usage of this cell to prototype a mixed latch- and flop-based design.

Acknowledgment

The authors would like to thank Ney Laert Vilar Calazans and the Accuser project for all support (process 401839/2013-3). Also, Alexandre would like to thank CNPq for the financial support (process 460205/2014-5).

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