Electrical Characterization of a C-Element with LiChEn

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***Abstract*—This demonstration presents the use of the Library Characterization Environment (LiChEn) for characterizing asynchronous standard cells. The tool was employed for the electrical characterization of a library with over five hundred asynchronous standard cells. In this work, a case study of a fundamental asynchronous component, the C-Element, will be presented to validate the use of the tool. LiChEn was designed due to the necessity of automating the process of characterizing asynchronous standard cells. Albeit this task can be done with tools from industrial EDA vendors, the use of these proved to require laborious manual work. These tools were designed for characterizing standard cells for synchronous systems and usually fail to recognize complex asynchronous logic. Moreover, asynchronous components are not available off the shelf in typical standard cell libraries, which constrains the asynchronous paradigm for full-custom approaches. As asynchronous techniques gain relevance in the research community, LiChEn can present a practical solution for a wider adoption of such techniques, by allowing an automated characterization of asynchronous standard cells.**

I. INTRODUCTION

According to the International Technology Roadmap for Semiconductors [1], a shift on the VLSI design paradigm is inevitable in future technology nodes with regard to clocking strategies. Thus, the use of asynchronous techniques [2] [3] is gaining relevance in the VLSI research community. Such techniques can be employed to guarantee correct communication between distinct frequency domains or even completely eliminate the clock signal of a chip or of some chip modules. Systems that employ different frequency domains with asynchronous interfaces to provide global communication are generically called globally asynchronous locally synchronous (GALS) [4]. Fully asynchronous circuits are more challenging and consequently are less often used. However there are some successful examples reported in recent literature, e.g. the Opus2 family of asynchronous DSP multiprocessors from Octasic Inc [5] and high speed FPGAs from Achronix, Inc.

Wider adoption of asynchronous techniques is constrained by the fact that such circuits still have limited design automation support [3]. There are a few tools for automating semi-custom asynchronous circuits design, but basic standard cells for implementing these circuits are not available off the shelf. In this way, asynchronous design is practically limited to full-custom approaches, where asynchronous logic components are specific to each design, and implemented through logic design approaches.

Building a generic standard cell library with components to support the asynchronous paradigm can be challenging. First, asynchronous circuits can be implemented using several different styles [3], each of which requiring a specific component set. Moreover, albeit typical industrial tools from vendors like Cadence, Mentor or Synopsys may be employed in the physical design of asynchronous components, the electrical characterization of such components using these tools is not straightforward. This is due to the fact that these tools aim primarily the synchronous paradigm. Characterizing sequential cells typically starts by treating control signals, especially the clock, and their assumptions. The drawback is that asynchronous sequential components are not controlled by a single global clock signal, but by signaling of specific, local events. Thus, using current commercial tools to characterize asynchronous cells entails laborious manual work.

This demonstration presents the use of the Library Characterization Environment (LiChEn), deemed to allow an automatic and precise electrical characterization process for asynchronous standard cells. LiChEn was developed to support any CMOS technology and is built around SPICE simulations. It allows the characterization of propagation and transition delays, internal and switching power, measured for different input slopes and output loads and modeled using non-linear table models. Also, it allows capturing input and output pins capacitance and the leakage power for each of the cell internal states and for each power source. LichEn was recently used to characterize the electrical behavior of cells in the ASCEnD library [6] [7], composed currently by over five hundred asynchronous components. In this demonstration, a typical standard cell for asynchronous circuits, the C-Element will be characterized with LiChEn.

II. THE C-ELEMENT

Asynchronous circuits can be implemented through a wide variety of templates [2] [3]. These templates usually rely on a delay model, a data encoding, a handshake protocol and a set of basic components at standard cell level.

A fundamental device that enables the design of several asynchronous templates is the C-element. The importance of C-elements is the fact that they help in the synchronization

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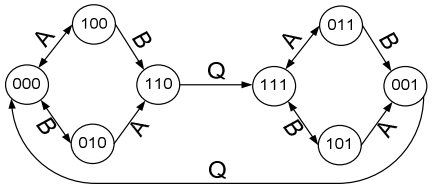
of independent events. Figure 1 (a) depicts the truth table and Figure 1 (b) shows a transition diagram for an ordinary 2-input C-element. Its output switches only when all inputs have the same logical value. When inputs A and B are equal, output Q assumes this same value. However, when inputs are different, the output keeps the previous logic value. The asynchronous state transition diagram of Figure 1 (b) for the C-element has vertices containing values of inputs and output in the order ABQ_i. Albeit this component can be build using typical logic gates available in most standard cell libraries, this is very inefficient.

A	B	Q_i
0	0	0
0	1	Q_{i-1}
1	0	Q_{i-1}
1	1	1

(a)



(b)

Figure 1 – Simple 2-input C-Element specification: (a) truth table and (b) asynchronous state transition diagram.

III. STANDARD CELL CHARACTERIZATION WITH LICHEN

LiChEn is implemented using the C/C++ language and is open source. It is based on the generation of a SPICE simulation environment where each standard cell has all its arcs and states exercised and its power and timing figures are characterized and exported to the Open Source Liberty format [8], compatible with most industrial EDA tools. The tool has no graphical interface and all commands are given through command line or a script file. The basic set of commands to perform a standard cell electrical characterization is given in this section.

In order to characterize asynchronous standard cells, the simulation environment must be configured. To do so, a technology is required, providing a corner, operating conditions, electrical specifications, and simulation parameters. First, technology models are furnished to the tool, together with the corner to use during the simulation. These are given with the commands "*set_models*" and "*set_process*", respectively. Next, the electrical parameters for collecting information are given as: minimum logical 1 and maximum logical 0 voltages, through commands "*set_vh*" and "*set_vl*". Also, low-to-high and high-to-low transition thresholds must be provided by the commands "*set_vlth*" and "*set_vhtl*".. The precision of the results generated by LiChEn for the provided technology depends on the quality of these parameters.

The tool also requires operating conditions, nominal voltage and temperature. These can be specified through the commands "*set_voltage*" and "*set_temp*". Global power nets also have to be informed through commands "*set_vdd*" and "*set_gnd*". Afterwards, parameters to control the simulation are given, such as the maximum simulation time "*set_sim_time*", the instant when to start measuring the information "*set_start_time*" and the simulation minimum step "*set_sim_step*".

Pin-to-pin propagation, transition delays and dynamic power consumption depend on the input slew rate and the output capacitance load. Hence, these delay and power figures are modeled in non-linear tables, where each value depends on a combination of an input slew rate and an output load capacitance. However, to do so, input slew rate and output load capacitance vectors are required, to generate the characterization simulation environment. These can be added through the commands "*add_slope*" and "*add_load*", respectively. These vectors can then be independently used to generate the models for each standard cell. Moreover, the quality of the results of a characterization based in non-linear table models is a function that strongly depends on the precision of the provided input slew rate and output load capacitance vectors.

Once the simulation environment is configured, standard cells can be provided to the tool. A SPICE netlist must be specified, containing the transistors schematic along with all parasitics. This can be done through the command "*add_*schematics". Also, the logic function of each standard cell, along with output and input pins names must be declared, to guide the tool when searching for transition arcs and static states, which will be used to conduct the simulations required for standard cells characterization. This is done using the "*add_cells*" command. In LiChEn, logic functions can employ the following logic operations: conjunction (*), disjunction (+) and complement (~). Moreover, parenthesis can be used to express hierarchy.

After added, cells must be bounded to model tables through the command "*add_model_table*". Only after a cell is added to the environment and bounded to a model (an input slew rate and an output load capacitance vectors), the command "*characterize_library*" can be issued. This command generates and simulates all scenarios required to characterize the standard cells. This includes finding all static states (SSs) and transition arcs and performing the characterization process based on the information given to the environment.

LiChEn may start the characterization process once all SSs and transition arcs have been computed. Based on these results, the tool generates SPICE files that implement each arc and each state. Measurements are conducted during SPICE simulation, which is triggered by the tool itself, based on the configuration given to the environment. During the characterization process, LiChEn measures input gate capacitance for low-to-high and high-to-low transitions, static and dynamic power and timing figures. Timing figures are measured as pin-to-pin propagation delays and output transition delays. The static power is measured for each SS. Dynamic power, in turn, is divided in two parts: switching and internal power, measured as the power consumed in DTAs and ITAs, respectively.

After modeling all the electrical figures of the standard cells of a library, LiChEn exports the generated results to a text based file according to the Open Source Liberty Format [8], which is compatible with most industrial EDA tools. This can be done by using the command "*export*".

IV. PROPOSED DEMONSTRATION

LiChEn was successfully used in the characterization of over five hundred C-Elements, basic components for asynchronous circuits. This demonstration will present the use of the tool to characterize one of these. The C-Element chosen for this demonstration is a two input symmetric Martin C-Element. The component will be characterized for a 65nm CMOS technology from STMicroelectronics for a typical process operating at nominal conditions using general purpose standard threshold transistors.

The LiChEn environment as well as all the steps and the commands issued during characterization will be presented. The obtained result, an Open Source Liberty Format file, can be used for timing and power analysis of an asynchronous integrated circuit and is compatible with tools from industrial vendors such as Cadence or Synopsys.

V. CONCLUSIONS

This demonstration will present an open source EDA tool for automatically characterizing asynchronous standard cell libraries. The tool is capable of characterizing input pins capacitance, static, internal and switching power and propagation and transition delays. Furthermore, it was efficiently employed in the electrical characterization of a standard cell library composed by over five hundred standard cells. As the interest in asynchronous circuits continuously grows in the research community, LiChEn can be very useful to enable semi-custom approaches to this design paradigm.

LiChEn is based on Cadence Spectre SPICE simulator. Future work includes allowing the use of other vendors' simulators. Another future work is enabling the tool to characterize multi output standard cells, which is very useful for specific classes of asynchronous circuits. A graphical interface is also part of future work, in order for the tool to be more user friendly. Another important thing about LiChEn is that it searches all SSs and transition arcs of a function, generating SPICE simulation scenarios, which can be very useful for academic purposes, such as microelectronics and VLSI design courses. Finally, LiChEn source code can be freely obtained by contacting the authors.

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