Bandwidth Efficient Gaussian Minimum Frequency-Shift Keying Approach for Software Defined Radio

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***Abstract*: This paper proposes a bandwidth efficient Gaussian Minimum Frequency-Shift Keying (GMSK) approach for software defined radio (SDR) platforms. The proposed demodulator applies a Gaussian filter with impulse response longer than the symbol period, which results in higher spectral efficiency. On the other hand, an impulse response longer than the symbol period causes inter-symbol interference (ISI), which may compromise the bit error rate (BER) performance. To address this issue, this paper proposes a new demodulation technique that takes into account the previous received bit at the demapping process. The proposed approach has been implemented and evaluated in Matlab and further described in VHDL and synthetized in a DIGILENT ZYBO ZynqTM - 7010 development board. Results show that the proposed method presents significantly reduced bit error rate when compared with other methods in the literature.**

***Index Terms*: SDR, CPFSK, DSP, DPLL.**

I. Introduction

Software Defined Radio (SDR) has been gradually replacing traditional implementation of communication devices by more flexible and cost effective ones. As is widely known, SDR is a radio technology in which most of the physical layer functions are implemented through software or firmware. The use of devices which are software controlled, such as field programmable gate arrays (FPGA), digital signal processors (DSP), general purpose processors (GPP) and programmable System on Chip (SoC), allow the configuration of several modulation waveforms in a single radio device.

Modulation techniques based on frequency-shift keying (FSK) are widely used in several wireless communication systems. For instance, continuous–phase modulation (CPM) is a good choice for nonlinear and band-limited channels [1]. The continuous phase characteristic is suitable for narrow bandwidth operation, and the constant envelope characteristic makes it particularly appealing for band-limited systems employing non-linear power amplifiers, such as satellite communication systems [2].

Among the continuous–phase modulations (CPM), Gaussian minimum shift keying (GMSK) is a particular spectrally efficient form of Minimum Shift Keying (MSK) widely used in GSM (Global System for Mobile Communications). Due to the continuous phase characteristic and narrow bandwidth, GMSK is appropriate for inter node communication links in Low Earth Orbit Satellite (LEO) constellations. The use of LEOs for internet access is an actual emerging trend. LEO constellations are able not only to provide access to internet services but also to provide fleet monitoring, border monitoring, agribusiness data-links and many other services in regions with poor communication infrastructure. Also for deep-space missions, the Consultative Committee for Space Data Systems (CCSDS) requires the exclusive use of GMSK for all interplanetary missions with transmission bit rates higher than 2 Mbps [3].

This paper proposes a new GMSK demodulation approach for SDR receivers. It adopts a Gaussian filter with impulse response longer than the symbol period in order to improve the spectral efficiency. However, a filter impulse response longer than the symbol period produces inter-symbol interference (ISI) [2]. To deal with this issue, this paper proposes a new demodulation approach that takes into account the previous received bit.

The GMSK modem has been simulated in Matlab and implemented in VHDL description language. VHDL implementation allows direct application of the proposed demodulator in SDR platforms. The results show that the proposed technique presents significantly superior performance when compared with similar methods available in literature.

II. Continuous Phase FSK Modulator

Fig. 1 shows a general block diagram of a Gaussian minimum shift keying modulator.

The input bitstream is applied to the mapper, which maps the stream of binary words of 1 bit into the respective sequence of symbols m_i at the mapper output. The symbols m_i are drawn from the set of two symbols $\Gamma = \{\pm 1\}$, which corresponds to the M=2 frequency levels of the GMSK modulation scheme.

The m_i symbols are up-sampled by a factor of N, where N represents the number of samples per symbol, and are applied to a rectangular window filter, where the N coefficients of the filter have unitary values. This process is represented by the resample block in the block diagram. The re-sampled symbols $r[n]$ are then applied to the Gaussian filter, with $B_G T$, where B_G is the bandwidth and T is the symbol period [4].

The sequence of filtered symbols $g[n]$ is applied to the phase memory block. In this block, $g[n]$ is multiplied by the constant value

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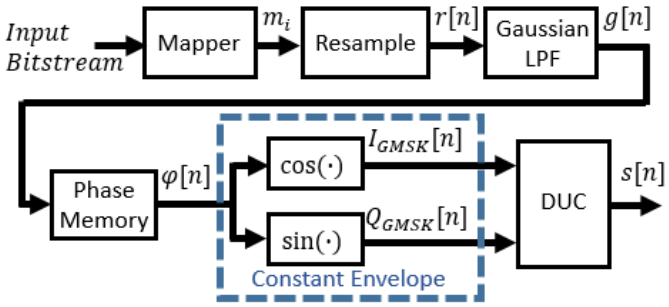

Fig. 1. GMSK modulator block diagram.

$$\varphi_{incr} = \frac{\pi . h}{N} \tag{1}$$

where h is the modulation index, which yields the modulation phase step $\gamma[n]$

$$\gamma[n] = g[n]\varphi\_incr \tag{2}$$

Subsequently the modulation phase step $\gamma[n]$ is smoothed by an integrator, thereby ensuring continuous transition between frequency levels at the constant envelope block that follows.

To this end, the phase memory block output

$$\varphi[n] = \gamma[n] + \varphi[n-1] \tag{3}$$

is applied to the input of the constant envelope block generating the in-phase and in-quadrature signals

$$\begin{aligned} \mathrm{I}_{GMSK}[n] &= \cos(\varphi[n]) \\ \mathrm{Q}_{GMSK}[n] &= \sin(\varphi[n]) \end{aligned} \tag{4}$$

The complex signal $s[n] = \mathrm{I}_{GMSK}[n] + j\mathrm{Q}_{GMSK}[n]$ is then applied to the *Digital Up Converter* (DUC) block in order to translate the generated baseband GMSK spectrum to the center frequency of the bandpass transmission channel.

III. Proposed GMSK Demodulator

Fig. 2 presents the block diagram of the proposed GMSK demodulator. The received signal $s'[n]$, applied to the demodulator input, is down converted by the Digital Down Converter (DDC) block and filtered by a low pass filter in order to remove the high frequency components, resulting in the complex baseband signal $x[n] = \mathrm{I'}_{GMSK}[n] + j\mathrm{Q'}_{GMSK}[n]$. In the sequence, the DDC output $x[n]$ is applied to the $arg(\cdot)$ block, responsible for computing the instant phase $\varphi'[n]$ of $x[n]$

$$\varphi'[n] = arg(\mathrm{I'}_{GMSK}[n] + j\mathrm{Q'}_{GMSK}[n]) \tag{5}$$

The differentiator block computes the phase difference $\varphi'_{Diff}[n]$, as follows

$$\varphi'_{Diff}[n] = \frac{\varphi'[n] - \varphi'[n-1]}{\varphi_{incr}} \tag{6}$$

$\varphi'_{Diff}[n]$ is then downsampled, thus remaining only one sample per symbol which is converted to the corresponding bit by the demapper.

The issue at this point is the inter-symbol interference caused by the Gaussian filter at the transmitter, which has an impulse response longer than the symbol period.

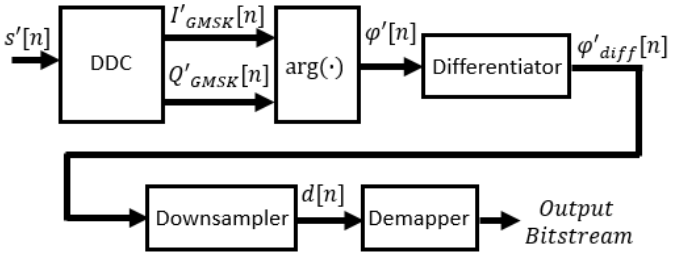

Fig. 2. Proposed GMSK demodulator block diagram.

Let us consider a noiseless channel. For a Gaussian filter with impulse response equal to the symbol period, the samples of the downsampler output sequence $d[n]$ assume values drawn from the alphabet set $\{+A, -A\}$ according to the transmitted bit value, 0 or 1. There is no symbol overlap in time for this case, as shown if Fig. 3, and the demapping process is easily implemented by means of a hard decision, which yields the demapper output bitstream $b_{out}[n]$ as follows:

$$\begin{aligned} &if \quad d[n] \geq 0, \quad then \quad b_{out}[n] = 1 \\ &else \qquad\qquad\quad b_{out}[n] = 0 \end{aligned} \tag{7}$$

Fig. 3(a) presents the input bitstream at the transmitter. Fig. 3(b) shows the differentiator block output $\varphi'_{Diff}[n]$ ('+'marks) and the downsampler output $d[n]$ ('o' marks) at the receiver. Observe that, for transmitted bit 1, the downsampler output is +1 and for transmitted bit 0, it is -1, considering a noiseless channel.

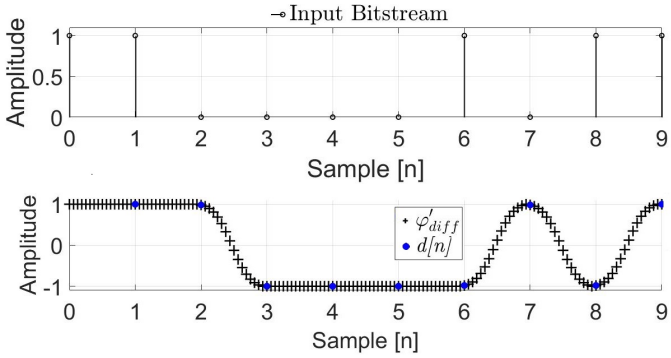

Fig. 3. (a) Bitstream applied to the modulator (b) Differentiator block output $\varphi'_{Diff}[n]$ ('+'marks) and downsampler output $d[n]$ ('o' marks) at the receiver, for a Gaussian filter with impulse response duration equal to one symbol period.

However, the proposed GMSK applies a Gaussian filter with impulse response longer than the symbol period. For this case, considering a noiseless channel, $d[n]$ samples may assume values drawn from the set $\{+A, 0, -A\}$ according to the present transmitted bit value and the previous transmitted bit value. For the pair of previous and present transmitted bits "11", $d[n]$ assumes $+A$ sample value. For the pair of previous and present transmitted bits "00", $d[n]$ assumes $-A$ sample value. For the pair of previous and present transmitted bits "01" or "10", $d[n]$ assumes zero sample value, as shown in Fig. 4. Fig. 4(a) presents the transmitted bitstreeam. Fig. 4(b) shows the differentiator output $\varphi'_{Diff}[n]$ ('+'marks) and the downsampler output $d[n]$ ('o' marks) at the receiver, for a

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Gaussian filter with impulse response duration equal to two symbol periods.

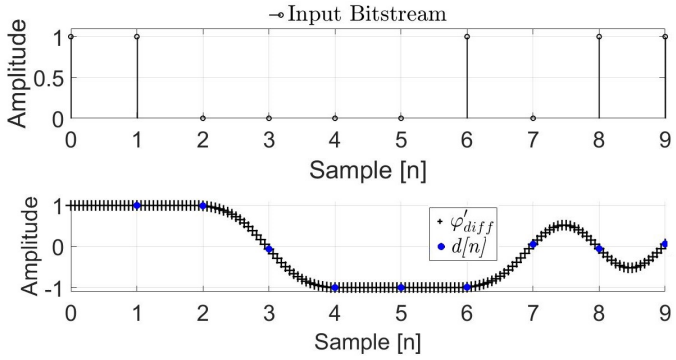

Fig.4. (a) Bitstream applied to the modulator (b) Differentiator block output $\varphi'_{Diff}[n]$ ('+'marks) and downsampler output $d[n]$ ('o' marks) at the receiver, for a Gaussian filter with impulse response duration equal to two symbol periods.

In order to address this issue, the proposed solution implements the demapper process by means of three decision regions:

$$\begin{aligned} &if \quad d[n] \geq +\frac{A}{2}, \quad then \quad b_{out}[n] = 1 \\ &else\ if \quad d[n] \leq -\frac{A}{2}, \quad then \quad b_{out}[n] = 0 \\ &else \qquad\qquad b_{out}[n] = \overline{b_{out}[n-1]} \end{aligned} \tag{8}$$

IV. Hardware Implementation

The proposed GMSK has been described in VHDL and implemented in a ZYBO ZynqTM - 7010 development board, manufactured by DIGILENT. The board integrates a dual-core ARM Cortex-A9 processor, with Xilinx 7-series FPGA logic.

The developed core is parameterized, allowing direct application in SDR platforms for GMSK waveform modulation. The GMSK demodulator is configurable for different Gaussian filter B_GT. The implemented architecture is based on 16 bits fixed-point arithmetic. Tables I and II show the FPGA resources required for the implementation of the GMSK modulator and demodulator, respectively.

TABLE I
FPGA RESOURCES REQUIRED FOR IMPLEMENTING THE GMSK MODULATOR

Resource	Available	Utilized	Utilization %
FFs	35200	116	0.33
LUTs	17600	616	3.5
BRAMs	120	1	0.83
DSP48s	80	19	23.0

TABLE II
FPGA RESOURCES REQUIRED FOR IMPLEMENTING THE GMSK DEMODULATOR

Resource	Available	Utilized	Utilization %
FFs	35200	106	0.30
LUTs	17600	1236	7.02
BRAMs	60	0	0
DSP48s	80	0	0

V. Experimental Results

In order to evaluate the proposed approach, modulator and demodulator have been implemented in Matlab and further described in VHDL. The results presented in this section considered $B_GT = 0.3$, 16 samples per symbol and Gaussian filter impulse response with duration of two symbol period. AWGN noise has been added to the modulated signal. Signal-to-Noise Ratio (SNR) of the AWGN channel is defined as

$$SNR = \sigma_S^2/\sigma_N^2, \tag{9}$$

where σ_S^2 is the variance of the transmitted signal and σ_N^2 is the variance of the noise.

Fig. 5 compares the performance results of the proposed approach with the results presented in [5]. It is possible to note that the proposed GMSK presents significant performance improvement. For SNRs above 15 dB, the proposed solution presents BER more than one order of magnitude lower than [5].

Fig. 6 compares the modulated signal PSD (Power Spectral Density) when considering the duration of the Gaussian filter impulse response equal to one symbol period and equal to two symbol periods. Note that the PSD for the Gaussian filter impulse response with same duration of the symbol period has larger bandwidth when compared with the case in which the Gaussian filter impulse response duration is two symbol periods.

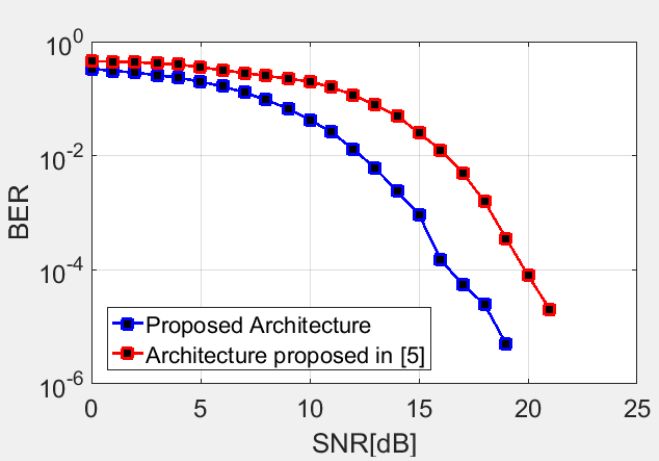

Fig. 5. Performance comparison: BER versus SNR.

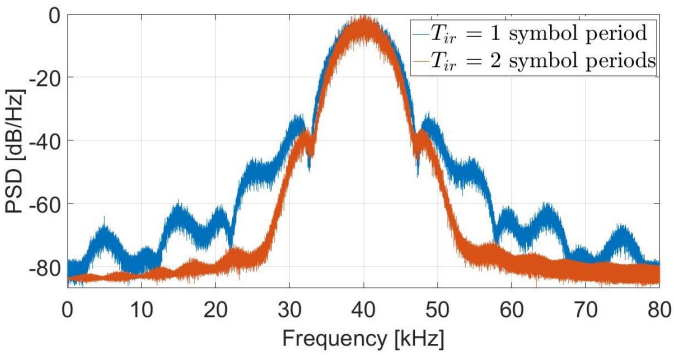

Fig. 6. Comparison of the Power Spectral Density for Gaussian filter impulse response duration T_{ir} equal to one and equal to two symbol periods.

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VI. Conclusion

This paper proposes a bandwidth efficient Gaussian Minimum Frequency-Shift Keying approach for software defined radio platforms. The proposed approach applies a Gaussian filter with impulse response longer that the symbol period, thus resulting in reduced bandwidth. The longer impulse response causes ISI, which is addressed in the demodulator by taking into account the previous received bit during the demapping process.

The proposed GMSK waveform for SDR has been implemented in VHDL and synthetized in a ZYBO ZynqTM - 7010 development board. The results indicate that the proposed solution presents significantly improved results. In terms of BER, the proposed demodulator presented improved results when compared with the architecture proposed by Kumar et. Al. [5]. Regarding the PSD, the bandwidth has been reduced in comparison with the Gaussian filter with impulse response duration of one symbol period.

The proposed approach is a good solution for narrow bandwidth applications that do not require high data rates.

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