Gate-Level Modelling of NBTI-Induced Delays Under Process Variations

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***Abstract*— Continuous technology scaling poses reliability concerns that directly affect the Integrated Circuit's (IC) lifespan. One of the most important issues in nanoscale circuits is related to the time-dependent variation caused by Negative Bias Temperature Instability (NBTI). Moreover, the impact of NBTI is exacerbated by Process Variation (PV), i.e. variations on transistor attributes during the manufacturing process. In this paper, a hierarchical model to compute NBTI-induced logic path delays at gate level considering PV is proposed. The model is applied in order to identify NBTI-critical logic paths of ICs that are subject to aging mitigation techniques. The model is derived based on intensive SPICE simulations of basic logic gates at transistor level under PV. The experimental results demonstrate an accurate fitting between the analysis performed on the proposed gate-level model and the electrical simulations, while the gate-level analysis provides for several orders of magnitude speed-up in simulation.**

Keywords — reliability, NBTI, PV, static timing analysis, aging, SPICE

I. INTRODUCTION

Continuous scaling of implementation technology has made lifetime reliability one of the key design factors to guarantee CMOS integrated circuit robustness. One of the most critical downsides of technology scaling beyond the 65nm node is related to the non-determinism of the devices' electrical parameters due to time-dependent deviations in the operating characteristics of the device. In [1] a brief overview of major sources of time-dependent variations is presented. Negative Bias Temperature Instability (NBTI) appears as one of the most important source of this type of variation and the major reliability issue when the gate oxide is thinner than 4 nm [2][3].

NBTI is a physical/chemical effect that occurs when a pMOS transistor is negatively biased and manifests itself as an increased threshold voltage V_{THp}. This results in drive current reduction and increased noise, which in turn causes a degradation of the device delay. V_{THp} degradation depends on time, voltage and temperature that means on circuit operation, which is difficult to predict. NBTI's effect on the long-term stability of functional logic may express itself through the incapability of computing in time the correct value at memory elements such as flip-flops due to the de-synchronization between clock distribution and signal propagation through the logic paths of a circuit. The de-synchronization effect is observed when the sum of all gate delays along a given path is larger than the time slack allocated by the designer for that path. When this condition occurs, the propagated signal reaches the memory elements at the end of the path in a time instant later than the clock front and, as a consequence, an incorrect value may be stored at that point of the circuit. The variation of V_{THp} of pMOS transistors due to dynamic NBTI (i.e. when the stress and recovery phases are iterating) is estimated to be 5-15% per year depending on the targeted technology and its environment [6][7]. The threshold voltage shift for devices at static NBTI (i.e. when a pMOS transistor is under constant stress) can be significantly higher. The path delay degradation follows the same trend, though with a smaller magnitude. It has been shown that NBTI depends on many factors [8] with strong correlation to the signal probability (P_z) (input duty cycle) and the output load capacity (C_L) [9].

Moreover, Process Variation (PV) has been pointed out as additional important issue to affect the circuit's reliability. Loosely, PV is caused by random fluctuations of dopant atoms affecting the device's electrical parameters and can be observed as a fixed deviation from the device's nominal behavior [17]. In this context, NBTI and PV have become the most prominent effects able to affect the circuit's V_{THp}. PV is hereby defined as the variation of the transistor attributes (length, width, oxide thickness) caused during the fabrication of the integrated circuits and manifests itself as V_{THp} variations, which results in variability in circuit performance and power. The impact of NBTI is exacerbated by PV, which makes the analysis of NBTI more complicated than other traditional reliability issues, as for example hot-carrier injection [3]. Two widely accepted theories exist, namely the Reaction-Diffusion model (R-D) [4] and Charge Trapping (CT)[5]. Both of them model the NBTI effect with some inaccuracy.

In this context, this paper proposes a NBTI model that takes PV into account and is based on SPICE simulations of individual gates under various PV parameters. In this paper, *mathematically convenient functions* for characterizing gate aging along the critical paths of logic circuits are applied, further, the gate and path delay degradation caused by NBTI aging are calculated. Derivation of such functions is based on SPICE-guided electrical characterization of logic gates. Experiments with an industrial ALU circuit demonstrate a good match between such gate-level approach and the electrical simulation results with the simulation speed-up of several orders of magnitude.

The remainder of this paper has been structured as follows: Section II presents an overview of works related to NBTI and PV. Section III describes NBTI effect modeling based on the dependence of the pMOS transistor threshold voltage shift $\Delta V_{THp}(x_i)$ on input signal probabilities P_z. Section IV introduces the process variation model, whereas Section V describes the proposed predictive models developed to characterize *NBTI-*

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induced gate delay degradation. As mentioned previously, these models are based on extensive Synopsys *HSPICE* simulations. Section VI presents experimental results and Section VII draws the final conclusions.

II. Preliminaries and Related Works

According to [17], pMOS V_{THp} can be affected by issues related to, both, NBTI and PV. In more detail, NBTI affects the circuits lifespan causing the degradation of the pMOS V_{THp} when a logic input equal to "0" is applied at the gate transistor. This negative bias leads to the generation of interface traps at the Si/SiO^2 interface. However, some of the interface traps can be eliminated by applying a logic input of "1" to the gate (recovery mode). Thus, NBTI degradation is directly dependent on the circuit's workload. Moreover, the silicon process also affects NBTI through Random Charge Fluctuation (RCF), which causes temporal variations. In more detail, V_{THp} degradation is subject to random fluctuations that increase as a function of stress time. Note that *static* NBTI is defined as such if only the structure utilization is considered, therefore not considering workload or temporal variations.

Furthermore, the circuit's degradation due to NBTI is exacerbated by PV. In more detail, PV can be categorized in two main groups: (1) inter-die and (2) intra-die variations [12]. Due to inter-die variations, the same device on a die can have different characteristics across various dies. However, due to intra-die variations, transistors can have different characteristics within a single die. Moreover, there are two more subcategories of intra-die variations: systematic and random variations. Systematic variations affecting transistors close to each other are expected to have relatively similar parameters, channel length and oxide thickness, when compared to those farther away on the die. Along with the variations due to NBTI, each device has also Random Dopant Fluctuations (RDF) associated to PV [17]. Due to RDF, transistors can have mutually independent V_{THp} variation with respect to each other, regardless of their spatial location. RDF is expected to be the major contributor to transistor V_{THp} variations in the sub-65nm technology [18].

Several works have been proposed in order to deal with NBTI concerns. Among them, [6] proposed an approach in order to alleviate the NBTI-induced aging effects in Static Random Access Memories (*SRAMs*). Another approach, [11], uses an experimentally verified NBTI model to study *DC* noise margins in conventional 6T *SRAM* cells as a function of NBTI degradation in the presence of PVs. Considering functional logic, the authors of [12] propose a transistor sizing technique that not only mitigates NBTI induced delay of the gate under consideration, but also minimizes its impact on the adjacent gates. This technique seems to be very effective, but it is mandatory to identify the critical gates and paths within the circuit in order to apply it. Otherwise, this technique would need to be applied to all the circuit gates, which would result in an unacceptable area overhead and eventually, excessive power consumption. In [13] the authors present a method characterizing the delay of every gate in a standard cell library as a function of the signal probability (P_z) of each of its inputs. Further, a technology-mapping technique that incorporates NBTI stress and recovery effects in order to ensure optimal performance of the circuit during its entire lifespan is applied. Although the calculation process in [9] and [13] is relevant as it allows the derivation of aging curves for logic components, it is also prohibitively time consuming. This is due to an extremely large number of stress-recovery cycles that have to be computed.

III. NBTI Effect Modeling

In the NBTI effect analysis, we model dependency of pMOS transistor threshold voltage V_{THp} shift on signal probability P_z. We rely on a combined model that takes into account a model proposed by Wang et al. in [9] for a predictive technology data and a model by Cao et al. proposed in [19] and supported by silicon measurements data. The work in [9] presents numerical values for *Predictive Technology Model* (*PTM*) 65nm technology [14], but lacks details regarding the extreme close-to-1 values for $P_z(x_i)$. Instead, it shows a discrete jump between dynamic and static V_{THp} degradations. On the contrary, the curve in [19] depicts a more realistic shape for close-to-1 $P_z(x_i)$ values.

Based on the combined data and formulae from [9] and [19] we have derived a curve depicted in Fig.1 that describes NBTI-induced pMOS transistor threshold voltage V_{THp} degradation dependency on signal probability $P_z(x_i)$ as a mathematically convenient function, where $P_z(x_i)$ is the signal probability for input signal x_i of a pMOS transistor in a gate. According to [9], in case of static NBTI, i.e. $P_z(x_i) = 1$, for PTM 65nm technology with the nominal values for environmental variables, after 10 years of NBTI-induced aging the upper limit of degradation is $\Delta V_{THp} = 0.27V$.

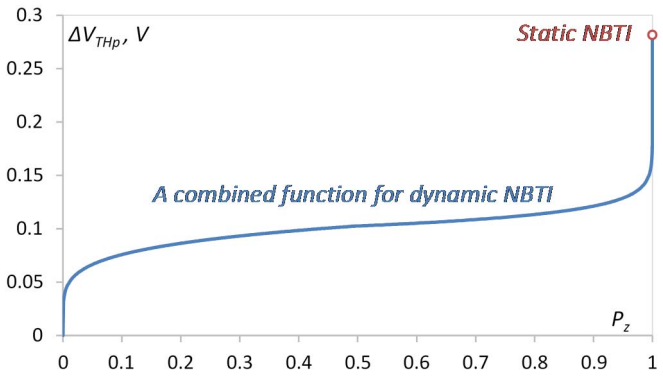

Fig. 1. Threshold voltage shift ΔV_{THp} as a mathematically convenient function of signal probability P_z (based on combined NBTI data from [9] and [19]).

Alternative technologies or alternative silicon measurements data may result in variations of the function shape. The data depicted in Fig. 1 allows fast computation of NBTI-induced pMOS transistor ΔV_{THp}, as it depends on a signal probability at the inputs of the considered logic gate. These voltage shift values serve as input values for modeling the NBTI-induced gate delays.

IV. Process Variation Modelling in SPICE

Accurate modeling of NBTI-induced gate delay degradation relies on intensive *SPICE* simulations. These simulations were performed using Synopsys HSPICE simulator. The 65nm Predictive Technology Model (PTM) [14] with a Vdd of 0.9V, a V_{THn} equal to 0.423V and a V_{THp} of 0.365V was adopted to

develop the proposed model. If a different technology is to be analyzed, the gate aging characterization procedure in SPICE has to be repeated.

The SPICE simulation step consisted of simulating the basic logic gates of the technology library for different pMOS transistor threshold voltage shift values (ΔV_{THp}). The goal was to capture the dependence of the gate output delay on the V_{THp}. The gates considered for simulation are the primitive Inverter, 2-input-NAND and 2-input-NOR.

The parameters chosen to be varied were transistor length (L), width (W), voltage threshold (V_{TH}), oxide thickness (t_{ox}), electron mobility (U_0) and temperature (T). All manufacturing parameters, except temperature, varied ±10% with a step of 5%, relative to the nominal values referenced in the PTM library and shown in Table I. The temperature varied from -40ºC to 140ºC with a step of 20ºC. Note, that no Monte Carlo simulation was performed with chosen parameters, because it was necessary to define boundaries (worst and best case) of possible impaction of PV on these parameters.

TABLE I. DESIGN PARAMETERS UTILIZED IN THE SPICE SIMULATIONS

65 nm TPM Library Parameters		
Parameter	NMOS	PMOS
V_{TH}, V	0.423	-0.365
t_{ox}, nm	1.85	1.95
U0, m²/(Vs)	0.0491	0.00574
T, ºC	27	27

Design Parameters						
Parameter	INV		NAND		NOR	
	N	P	N	P	N	P
W, nm	27	51	54	51	27	102
L, nm	60	60	60	60	60	60

For each gate, the impact of PV on each parameter was first evaluated. For the 2-input-NAND and the 2-input-NOR, the influence of different combinations for input pins (i.e., "AB" = "00", "01", "10", "11") was evaluated. Taking into account that NBTI degrades pMOS transistors, the output gate transition under consideration was 0→1. It the paper we consider that all pMOS transistors are degraded at the same rate. All observed delays were compared against the delay of a fresh gate (without degradation), which did not suffer from any process variation. The gate output delay degradation in percent of (a) gates affected by both process variation and NBTI degradation compared to (b) the golden model was calculated.

Each graph contains five curves that represent different degrees of PV, i.e. -10%, -5%, 0% (without PV), +5%, +10%. The *x-axis* represents the difference of V_{THp} in Volts between the analyzed NBTI-induced gate under PV and the nominal reference from a non-aged gate. The *y-axis* represents the delay degradation (Δt) in percent of the analyzed gate compared to the golden model operating at nominal temperature. Thus, a negative Δt represents gate delay decrease, while positive Δt indicates gate delay degradation due to PV and NBTI effects.

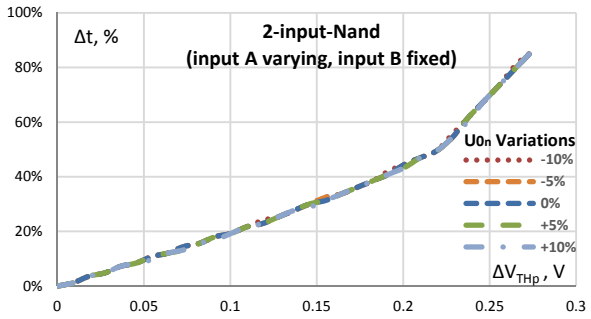

Fig. 2. Gate delay degradation Δt as a function of ΔV_{THp} and U_{0n} variation

The simulations for varying $U0_n$ have demonstrated that this parameter causes little or no impact on the gate output delay. This is due to the fact that the variation boundaries defined here are not able to cause a sensitive delay degradation. Furthermore, the intrinsic majority carrier (i.e. electrons) mobility in the nMOS is much higher than in pMOS transistors, which is not enough to provoke a significant influence on delay. The respective results are illustrated in Fig. 2. Similar results were obtained by simulating PV for both V_{THn} and t_{oxn}.

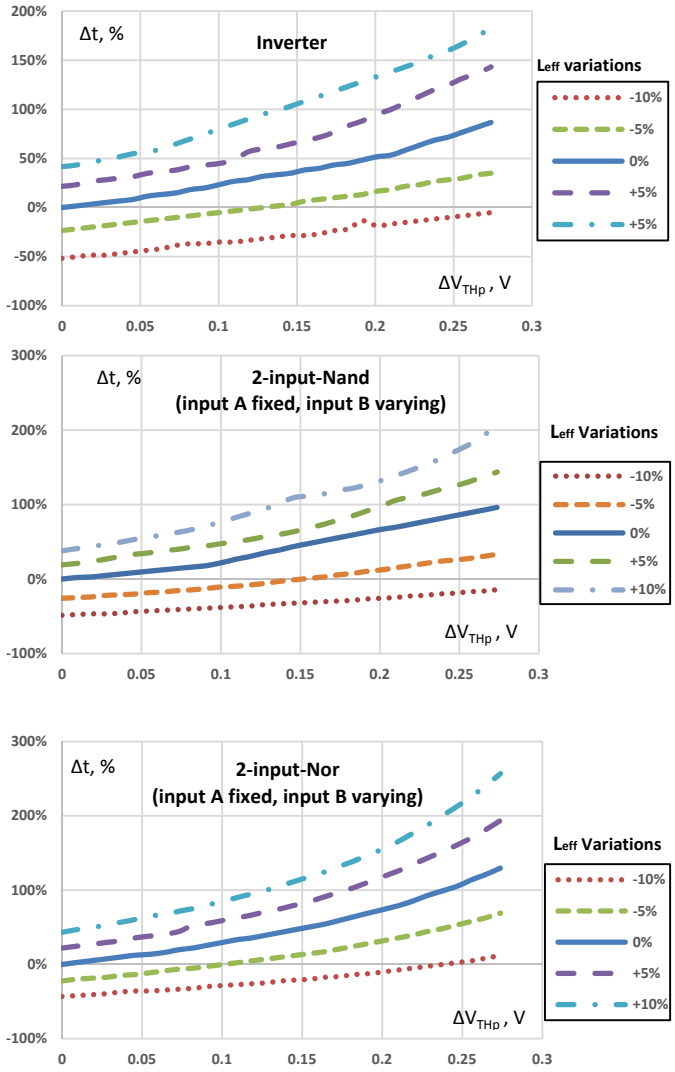

Fig. 3. Gate delay degradation Δt as a function of ΔV_{THp} and L_{eff} variations

The variation of parameters L_{eff}, W_{eff}, V_{THp}, t_{oxp}, $U0_p$, and T have induced a large range of gate delay degradation. When comparing the impact of L_{eff} parameter on all gates, it is possible to observe that smaller lengths imply not only on faster transistors, but also on smaller time degradations caused by aging, as shown in Fig. 3.

For the *2-input-NOR* gate delay graph shown in Fig. 3, it is possible to state that after 0.25V ΔV_{THp} degradation, the -10% L_{eff} variation curve presents no time degradation when compared to a nominal reference, interpreted to as no PV and no NBTI degradation. Such nominal reference curve presents almost 75% delay variation under the previous level of threshold degradation, and the +10% L_{eff} Variation curve presents an even larger up to 250% delay degradation. Such differences on delay occur due the effect of L on the electrical channel formed below the oxide of transistors. It is important to note that all the variations on these parameters unbalance the gates. In other words, the gates no longer take the same amount of time to perform their transitions (0→1 and 1→0).

Fig. 4 illustrates the results of varying V_{THp} values, which exhibits significant impact caused by PV on both initial values and degradation curves. It is also important to stress that different degrees of PV achieve different degrees of ΔV_{THp}, which does not happen with other parameters. Such fact is explained by the NBTI model adopted in this work, which consists of voltage sources connected directly to pMOS transistors that emulate the effect of aging based on the threshold voltage shift of the pMOS transistor. Therefore, greater variations of V_{THp} caused by PV, will result in larger degradation effects (both ΔV_{THp} and Δt) caused by NBTI.

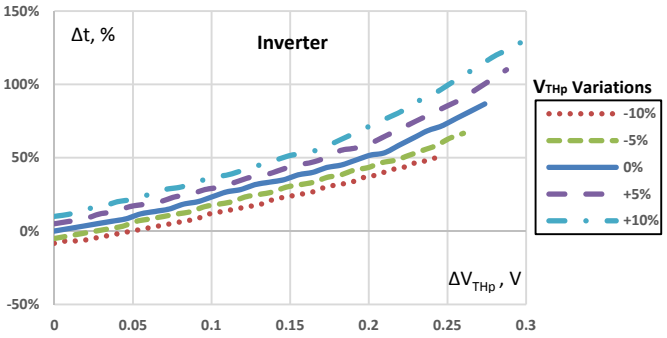

Fig. 4. Gate delay degradation Δt degradation as a function of ΔV_{THp}

The remaining parameters (W_{eff}, t_{oxp}, and $U0_p$) are discussed below. The parameter W_{eff}, shown in Fig. 5, caused a perceptive, but low variation compared to initial delay values on all gates and maintained as a constant delay degradation. The t_{oxp} variation have low, but remarkable impact on delay degradation. The parameter $U0_p$ in general has a great alteration on delay with signs of a linear delay degradation.

After all parameters were individually analyzed, a setup where all significant design parameters (L_{eff}, W_{eff}, V_{THp}, t_{oxp}, and $U0_p$) were varied at the same rate was considered. These simultaneous variations were evaluated under three situations: T=140°C (worst case), T=27°C (nominal), and T=-40°C (best case). In all cases, the gate with no PV at nominal temperature was set as reference value. The others curves represented in the graph have their parameters varied as mentioned before. It is also important to note that the V_{THp} parameter is varying due to PV and the degrees of ΔV_{THp} caused by NBTI will also vary from curve to curve. These curves are illustrated in Fig. 6.

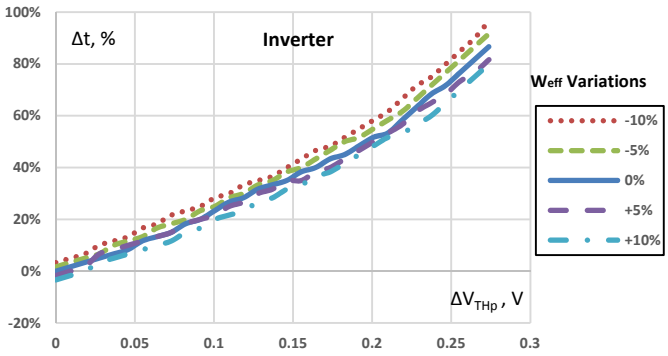

Fig. 5. Gate delay degradation Δt as a function of ΔV_{THp} and W_{eff} variation

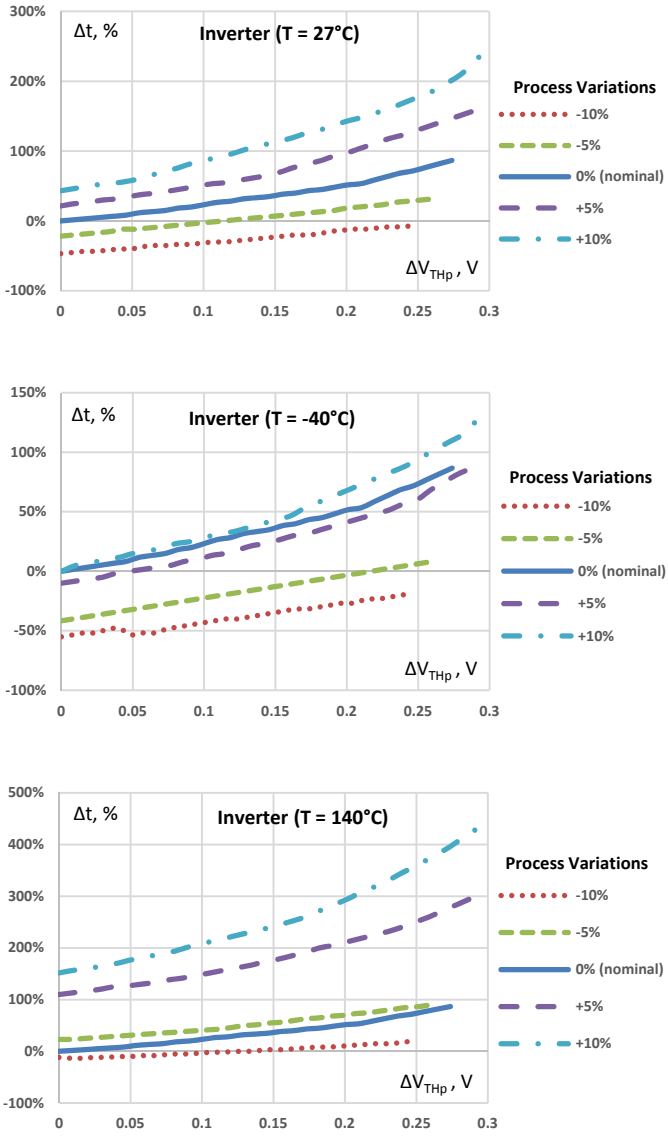

Fig. 6. Gate delay degradation Δt for an Inverter as a function of ΔV_{THp} for different process variation parameters and operation at diffent temperatures

Two distinct behaviors have been observed when the nominal curve (T=27°C) was compared to the T=-40°C and T=140°C curves. First, when analyzing only curves from the T=-40°C (best case) scenario, it is possible to conclude that gates with positive variations are prone to suffer degradations similar to a new gate operating under nominal temperature. While gates with negative variations, although impacted by ΔV_{THp}, do not present significant degradations on delay caused by NBTI. The opposite behavior was observed when analyzing the curves from the T=140°C (worst case) scenario. Gates that suffered negative PV exhibited similar curves to the nominal reference, characterizing a small impact on both ΔV_{THp} and Δt. However, gates that suffered positive PV show greater levels of delay degradation: 300% Δt for +5%, and almost 450% Δt for +10%.

V. NBTI-induced Gate Delay Degradation Modelling Under process variation

According to [9], the maximum possible threshold voltage shift can be achieved when a pMOS transistor is under static NBTI and it equals to 0.27V for 10-year induced NBTI aging. Therefore, SPICE simulations have been performed increasing the $\Delta V_{THp}(x_i)$ value step-by-step from 0V to 0.27V. A small 2.5% sampling step was applied to guarantee smooth and continuous curves.

Fig. 7 shows the gate-aging characterization curve (without PV at nominal T=27°C) in SPICE for an Inverter. It captures the dependence of the gate output delay on ΔV_{THp} for the rising input transition 0→1. The following mathematically convenient function (black dash curve) was matched to the curve characterized with SPICE (blue curve) in order to extract gate output delay dependency on NBTI-induced aging due to ΔV_{THp}:

$$\Delta t_{gate} = \lambda \cdot \Delta V_{THp}(x_i) + \mu \cdot \Delta V_{THp}(x_i)^2 \quad (1)$$

where Δt_{gate} is the gate output delay increase in percent compared to nominal gate delay, $\Delta V_{THp}(x_i)$ is the change of threshold voltage V_{THp} for pMOS transistors at the gate input x_i. λ and μ are technology dependent constants, whose values determine the type of gate, number of inputs, the input number where particular 0→1 or 1→0 transition takes place, and PVs considered, i.e. the shape of a curve.

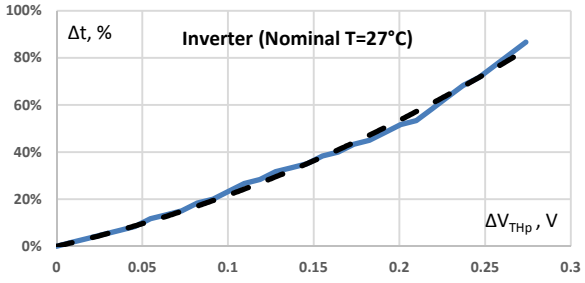

Fig. 7. Dependence of gate output delay on V_{THp} shift in SPICE (blue) and the function (black dash) that matches the SPICE results for Inverter gate.

As the result of extensive electrical simulations of individual gates in SPICE considering different PV parameters, this work extracts a list of λ and μ values that define gate output delay degradations under various conditions. These values are used to precisely model NBTI-induced path delay degradation under PVs.

VI. NBTI-induced Path Delay Degradation Identification Under Process Variation

The approximation of the SPICE curves gained at the transistor-level to mathematically convenient polynomial equations proposed in Section V enables fast hierarchical identification of NBTI-critical logic paths at the gate-level as well as under considered PVs. It is based on simulation of input stimuli and utilizing received signal probabilities P_z in statistical static timing analysis with nominal gate delays and calculating the longest NBTI-degraded paths using NBTI-induced path delays.

An *NBTI-critical path* [20] is a path in the circuit whose NBTI-induced delay degradation exceeds the initial time slack allocated by a designer, i.e. the path becomes delay-critical path. The *longest NBTI-degraded path* is the path that has the total longest delay when considering NBTI-induced additional delays Δt for the gates along that path. Here, NBTI-critical paths have to be analyzed both for 0→1 and 1→0 transitions at their primary inputs since gates being under NBTI-stress (0→1 transition at gate input) are alternating along the path.

NBTI-critical paths are identified applying an approach presented in [15] where for each consequent gate in the circuit are determined a set of ingoing paths which proceed to the next gate. To avoid an explosion of the number of paths to be analyzed, a threshold is introduced to limit the number paths to be traced up. As a result, for each primary output a set of NBTI-critical paths is obtained. Further, these can be used for NBTI mitigation techniques (e.g. [20]).

VII. Experimental Results

NBTI-critical paths identification under PVs is demonstrated on a 4-bit ALU 74HC/HCT181 design from Philips [16] with minor modifications introduced, i.e. the XOR gates are substituted by NAND and Inverter gates. It is a gate-level combinational logic design, where primary inputs and outputs are connected to the flip-flops.

First, to enable NBTI effect modelling, for all pMOS transistors that are extracted from gate-level netlist of given ALU input signal probabilities P_z are calculated by simulating all input stimuli combinations. Second, these values are used as an input to compute the ΔV_{THp} values for pMOS transistors by using the data from Fig.1. The resulted ΔV_{THp} values serve as an input for Equation (1) to model NBTI-induced gate output delay degradations under different PV parameters based on SPICE simulations. Finally, to indicate how a set of possible PV parameters can impact positively (decrease delay) or reinforce NBTI-induced path delay degradation.

In our experiment, the same 5 NBTI-critical paths leading to various outputs have been selected as in [10]. In Table 2 are shown delay degradations Δt in percent for 0→1 and 1→0 transitions at primary outputs for considered paths in case of NBTI-induced aging and under PVs at nominal temperature 27°C. Nominal delays in *ns* of given paths were obtained as a result of SPICE simulations. -5% PV (+5% PV) means that all significant design parameters: L_{eff}, W_{eff}, V_{THp}, t_{oxp} and $U0_p$ were changed simultaneously by -5% and +5% correspondingly. The possible influence on path delay degradation was evaluated by the proposed approach based on SPICE simulation of individual gates under considered PVs. The values in columns -5% PV

and +5% PV indicate possible range of NBTI-induced path delay degradation deviation from nominal delay due to indefinite variations in process parameters.

TABLE II. NBTI-INDUCED PATH DELAY DEGRADATION UNDER CONSIDERED PV PARAMETERS

Path	0->1 transition				1->0 transition			
	Nominal delay t, ns	delay degradation Δt, %			Nominal delay t, ns	delay degradation Δt, %		
		NBTI	-5% PV	+5% PV		NBTI	-5% PV	+5% PV
F3#26	228.6	14.7	-8.7	39.8	216.9	13.4	-8.9	36.8
F3#38	207.0	13.8	-8.9	37.6	205.8	14.1	-8.6	38.0
F2#61	205.3	13.1	-9.4	37.2	199.1	14.7	-8.4	38.9
F3#74	211.4	14.2	-8.7	38.5	222.6	14.6	-8.2	38.6
F1#77	149.1	8.6	-11.7	30.1	159.1	19.6	-6.8	48.2

Fig. 8 shows the same data from Table 2, but demonstrates how an identification of NBTI-critical paths may be complicated under PVs.

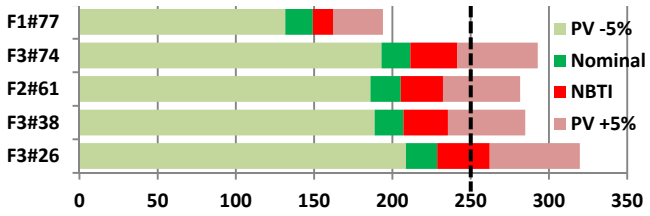

Fig. 8. An impact of PVs on NBTI-critical path identification

Assume the maximum allowed delay for given paths is 250 *ns* (vertical dashed line). Nominal delays (right side of dark green) do not exceed it. However, due to NBTI effect path F3#26 becomes NBTI-critical (right side of red) since its delay degradation overcomes the allowed delay. Nevertheless, PVs may mitigate delay degradation and even decrease it compared to nominal one (right side of light green). On the other side, negative effect of PVs may increase delay degradation of paths F3#74, F2#61 and F3#38 (right side pink) and change them to NBTI-critical ones. By varying the temperature value the possible range of considered PVs impact can be significantly expanded as shown for Inverter gate in Fig. 6.

The NBTI-induced delay degradation simulation time for each path is about 1 minute (excluding settings tuning time) in HSPICE compared to the proposed gate-level analysis which requires only 0.5 seconds of CPU time (Dual core 2.2 GHz, 4GB RAM) for simulation of all *NBTI*-critical paths under considered PV parameters. Thus, the speed up of NBTI modeling for the proposed approach is at least by 100 times.

VIII. CONCLUSIONS

One of the dominant reliability concerns today is the NBTI effect in 65nm implementation technologies and below, which is exacerbated by process variations on transistor attributes during the manufacturing process. This paper, first, has presented a set if intensive simulations with HSPICE from Synopsys for NAND, NOR and Inverter basic logic gates at the transistor level under PV and corresponding analysis of the PV impact on the gate nominal delay and the delay degradation. Second, based on these simulations, it has proposed a hierarchical model to compute NBTI-induced logic path delays at gate-level under consideration of process variations. Third, the model was applied to identify NBTI-critical logic paths in the circuit considering PVs with a gate-level analysis, thus achieving order of magnitude speed-up compared to an analysis at the transistor-level.

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