**Current Saturation** 



## Anomalous Current–Voltage Behavior in Al/TiO<sub>2</sub>/n-Si Structures

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The current–voltage (J–V) curves of Al/TiO<sub>2</sub>/n-Si structures present an anomalous behavior where the current becomes constant for a reverse bias higher than  $\approx$ 0.65 V. Here we analyze devices fabricated by spin-coating of an organometallic precursor and subsequent annealing in an O<sub>2</sub> atmosphere. The details of the current saturation phenomenon are interpreted as a consequence of the formation of a depletion region in Si, which limits the voltage drop in the film and truncates the current. The analysis is supported experimentally by capacitance–voltage and photoconductance measurements. It is also shown that the saturation current can be controlled by modifying the film's deposition conditions, changing the barrier for electron injection from Al to TiO<sub>2</sub>.

The current-voltage (I-V) characteristics of heterostructures are determined by bulk conduction through each material and the bands' energy alignment of each interface. In the case of TiO<sub>2</sub> contacted by low work-function ( $\approx 4 \, \text{eV}$ ) metals, conduction is usually limited by bulk transport in TiO<sub>2</sub> by the space-chargelimited-current (SCLC) mechanism<sup>[1,2]</sup> due to easy electron injection from the contacts and a low conductivity of TiO2.[3-5] This structure behaves like a leaky capacitor, since there is charge transport occurring during steady-state operation. The difference from a regular capacitor, besides the very high leakage current, is that the negative charge is not accumulated in one of the capacitor plates but instead is distributed throughout the titania. The study of these conduction aspects in TiO<sub>2</sub> is now becoming important given its active role in semiconductor devices such as solar cells (including dye-sensitized<sup>[6]</sup> and perovskite<sup>[7,8]</sup>), resistive memories,<sup>[1,9]</sup> MIS capacitors employing high- $\kappa$  dielectrics<sup>[10]</sup> and even transparent conducting oxides,<sup>[4,11]</sup> to list a few. Recently the TiO<sub>2</sub>/ Si heterojunction was used as a solar cell,<sup>[12–15]</sup> taking advantage of the hole blocking capabilities of TiO<sub>2</sub>.

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Here we report an unusual *J*–V behavior, shown in Figure 1, that was found when we used n-type Si instead of a metal as one of the capacitor plates, forming an Al/TiO2/n-Si structure. At first sight, this *I*–*V* curve may seem odd, because the barrier for injection from metal to semiconductor or from semiconductor to metal is very  $\mathrm{low}^{[12,13,16]}$ (see Figure 1b and c) and the current should be limited only by bulk conduction through titania. In this case the structure should behave like a non-ohmic resistor because of the SCLC mechanism.<sup>[13,16]</sup> Indeed for positive voltages on Al (forward bias) this is the observed behavior. On the other hand, for negative voltages on Al (reverse bias) this

behavior is observed only up to about 0.65 V. For biases higher in magnitude than this value, the current becomes saturated. The phenomenon was actually observed in reports by Man et al.,<sup>[16]</sup> Laha et al.,<sup>[17]</sup> and Brown and Grannemann<sup>[18]</sup> for TiO<sub>2</sub> deposited by chemical vapor deposition, sputtering and electron-beam evaporation, respectively, but no thorough analysis was given. The purpose of this work is to give a convincing explanation for this anomaly.

In our samples, the  $\approx 20$  nm thick TiO<sub>2</sub> layer was deposited at room temperature by spin-coating of the organometallic precursor titanium diisopropoxide bis(acetylacetonate) diluted in isopropanol at 3000 rpm and 30 s. Concentrations of 0.15 and 0.30 M were tested. The samples were then dried in a hot plate at 125 °C in air for 10 min and subsequently annealed in an O<sub>2</sub> atmosphere for 30 min (the annealing temperatures varied from 420 to 540 °C). The substrate was a low resistivity (0.01 cm) n-Si wafer with a 60 µm thick n-Si epitaxial layer of 20 cm ( $N_D = 2 \times 10^{14}$  cm<sup>-3</sup>) cleaned with a piranha solution followed by an HF dip. The Al electrode was deposited in the form of disks with 100 µm radius and ≈500 nm thickness by thermal evaporation. The (ohmic) back contact was an eutectic InGa alloy.

To understand the reason for the current saturation, consider the leaky capacitor structure but with n-type Si instead of a metal as one of the contacts and Al as the other electrode. For no applied voltage, the semiconductor surface is in accumulation, caused by the metal-semiconductor work function difference and some amount of fixed positive charges in titania. The flatband voltage,<sup>[19]</sup>  $V_{FB}$ , is negative:

$$V_{\rm FB} = \phi_{\rm m} - \phi_{\rm s} - \frac{Q_{\rm f}}{C_{\rm ox}} < 0 \tag{1}$$





**Figure 1.** a) Typical *J*–V behavior of an Al/TiO<sub>2</sub>/n-Si structure showing a current "saturation" for reverse biases higher than  $\approx$ 0.65 V (negative in aluminum). The equation is for a power law fit in the region before saturation. The band diagrams are for (b) forward bias in accumulation and (c) reverse bias in depletion.

because the metal work function,  $\phi_{\mathrm{m}}$ , is lower than that of the semiconductor,  $\phi_s$ , and because the fixed charges in the film,  $Q_{\rm f}$ , are positive.  $C_{\rm ox}$  is the oxide capacitance. Now, if a negative voltage lower in magnitude than the flatband voltage is applied in aluminum with respect to silicon, electrons will start to flow via the SCLC mechanism, but the semiconductor surface will remain in accumulation. Since in accumulation the charge in Si varies as  $\approx \exp(\psi_s)$ , where  $\psi_s$  is the voltage drop in Si, and the charge in TiO<sub>2</sub> varies as  $\approx V_{\text{TiO}_2}$ , where  $V_{\text{TiO}_2}$  is the voltage drop in the film, charge neutrality in the device dictates that most of the applied voltage will drop in the oxide. In this case the current through the device is given by a SCLC power law  $I \sim (V_{\text{TiO}_2})^n$ , where *n* is equal to or higher than 2, depending on the distribution of defects in titania.<sup>[20]</sup> This is indeed the observed dependence for voltages less than the voltage at which the current is truncated, as shown by the power law fit in Figure 1a.

For applied voltages, V, higher in module than  $|V_{\rm FB}|$ , a depletion layer containing positive charges will start to build up in Si to balance the negative charges accumulated in titania and maintain charge neutrality. This time, however, a significant voltage drop in Si will result, because in depletion  $Q_{\rm d} \sim \sqrt{\psi_{\rm s}}$ , where  $Q_{\rm d}$  is the positive charge in the depletion region, while the charge in titania is still given by  $Q_{\rm t} \sim V_{\rm TiO_2}$ , where  $Q_{\rm t}$  is the negative charge distributed in the film. Using the charge neutrality condition one can obtain  $V_{\rm TiO_2}$  and  $\psi_{\rm s}$ :



$$Q_{t} = Q_{d}$$

$$\frac{9}{8} \frac{\varepsilon_{t} A}{d} V_{\text{TiO}_{2}} = A \sqrt{2q \varepsilon_{s} N_{D} \psi_{s}}$$

$$V_{\text{TiO}_{2}} = K \sqrt{\psi_{s}} = K \sqrt{V - V_{\text{FB}} - V_{\text{TiO}_{2}}}$$
(2)

where *q* is the proton charge,  $\varepsilon_s$  ( $\varepsilon_t$ ) is the static dielectric constant of Si (TiO<sub>2</sub>), *A* is the electrode area, *d* is the film thickness, and  $K \equiv (8d/9\varepsilon_t)\sqrt{2\varepsilon_sqN_D}$ . The factor of 9/8 comes from the fact that the negative charge of the capacitor is not concentrated in a plate but instead is distributed throughout a volume, making the average distance between the two plates of the capacitor slightly smaller and the capacitance slightly larger.<sup>[20]</sup> Solving Equation (2) for the voltage in TiO<sub>2</sub> and in Si, one obtains

$$V_{\text{TiO}_2} = \frac{K^2}{2} \left( \sqrt{1 + 4\frac{(V - V_{\text{FB}})}{K^2}} - 1 \right) + V_{\text{FB}}$$
(3)

$$\psi_{\rm s} = \frac{K^2}{2} \left( 1 + 2 \frac{(V - V_{\rm FB})}{K^2} - \sqrt{1 + 4 \frac{(V - V_{\rm FB})}{K^2}} \right) \tag{4}$$

Note that Equations (3) and (4) are only valid for voltages higher in magnitude than the flatband voltage. Overall,  $V_{\text{TiO}_2} \approx V$  and  $\psi_{\text{s}} \approx 0$  for  $|V| < |V_{\text{FB}}|$  and  $V_{\text{TiO}_2} \sim \sqrt{V}$  and  $\psi_{\text{s}} \sim V$  for  $|V| > |V_{\text{FB}}|$ . The resulting behavior is plotted in **Figure 2** for  $K = 5 \times 10^{-3} \text{ V}^{1/2}$ , a value obtained using  $\varepsilon_{\text{s}}/\varepsilon_0 = 11.7$ ,  $\varepsilon_{\text{t}}/\varepsilon_0 = 30$ , d = 20 nm, and  $N_{\text{D}} = 2 \times 10^{-4} \text{ cm}^{-3}$ .

This explains why the current through the structure saturates. Once the flatband voltage is reached, the "excess voltage"  $V - V_{FB}$  will stop being mostly dropped in the film because of the formation of a depletion region, and the current will stop increasing. Additionally, from Equation (2) and the low value of  $K \approx 10^{-3}$  one can see that the excess voltage drop in titania is actually negligible in comparison to that in silicon (at least three orders of magnitude lower) after the depletion layer starts to build up. This is why V<sub>TiO2</sub>, and consequently J, becomes constant beyond  $V = V_{FB}$ . The structure then behaves as a current source. Note that for higher values of K the voltage drop in titania could become appreciable even when the semiconductor is in depletion, as shown in Figure 2 for  $K = 0.5 V^{1/2}$ . Higher values of K could be obtained with higher doping levels of the semiconductor or with films with lower dielectric constants and higher thicknesses.

One might expect that at the onset of strong inversion the depletion layer width should stop increasing and the current should start increasing again. However, we argue that strong inversion is actually never reached in this structure. This is because the amount of electrons injected from Al through the titania is many orders of magnitude larger than the amount of holes thermally generated forming the inversion layer. Even if the lifetime in Si is as low as  $1 \,\mu s$ , a simple estimation<sup>[19]</sup> puts the generation current at about  $10^{-4} \,\mathrm{mA \, cm^{-2}}$ , which is still at least three orders of magnitude lower than the truncated current observed in Figure 1a. This means that holes recombine with the injected electrons before they can form the inversion layer, and the semicondutor is kept in deep depletion.







**Figure 2.** Plot of voltage drop in TiO<sub>2</sub> and in Si versus applied voltage for  $K = 5 \times 10^{-3} V^{1/2}$  (solid lines) and  $K = 5 \times 10^{-1} V^{1/2}$  (dashed lines).

To confirm these hypotheses, we show in **Figure 3** the region of interest of a typical capacitance–voltage (*C*–V) curve for this structure measured at 1 kHz. A low frequency is necessary to avoid errors caused by the high conductance of our samples.<sup>[21]</sup> The Debye length for our Si substrate is<sup>[19]</sup>  $L_{\rm D} = \sqrt{kT\varepsilon_{\rm s}}/N_{\rm D}q^2 = 289$  nm, corresponding to a capacitance of  $\varepsilon_{\rm s}A/L_{\rm D} = 11.3$  pF, and the measured oxide capacitance (not shown) is  $C_{\rm ox} \approx 400$  pF, giving a capacitance at flatband,  $C_{\rm FB}$ , of

$$C_{\rm FB} = \left( \left( \frac{\varepsilon_{\rm s} A}{L_{\rm D}} \right)^{-1} + C_{\rm ox}^{-1} \right)^{-1} \approx 10 \text{ pF.}$$
(5)

In the *C*–*V* curve this capacitance corresponds to 0.6 V, in very good agreement with the voltage at which current saturation occurs in Figure 1a. It is noted that the flatband capacitance is almost equal to the minimum capacitance because of the low doping in these samples, which gives a relatively high Debye length. The hypothesis of deep depletion can also be confirmed from the *C*–*V* curve for voltages higher in module than 0.7 V, as



**Figure 3.** Portion of the C–V curve of Al/TiO<sub>2</sub>/n-Si structures showing the flatband capacitance at V = 0.6 V. The inset shows the deep depletion region of the same plot.

shown in the inset of Figure 3. The voltage at which strong inversion should occur  $\mathrm{is}^{[19]}$ 

$$V_{\rm FB} - \frac{A\sqrt{2\varepsilon_{\rm s}qN_{\rm D}2\phi_{\rm F}}}{C_{\rm ox}} - 2\phi_{\rm F} = -1.1 \text{ V}$$

$$\tag{6}$$

where  $\phi_{\rm F} = kT/q \ln(N_{\rm D}/n_{\rm i})$  and  $n_{\rm i}$  is the intrinsic carrier concentration in Si. However, the capacitance continues decreasing for higher voltages (in module), in agreement with the deep depletion hypothesis.

It was also found that the saturation current can be reproducibly controlled by changing the precursor concentration and the annealing temperature of titania. In Figure 4, we show six I-V curves for films annealed in O2 at three different temperatures (420, 480, and 540 °C) and deposited with two different concentrations of the organometallic precursor (0.15 and 0.30 M). The dependence is quite clear: higher annealing temperatures and higher precursor concentrations lead to lower saturation currents. At first, one might try to explain this dependence with the presence of a SiO<sub>2</sub> layer grown during the annealing step. However, note that a temperature of 540 °C is too low to grow a significantly thick SiO<sub>2</sub> layer. We therefore expect that the thickness of the interfacial layer is that of a native oxide independently of temperature, which means it cannot be the cause of different saturation currents for different samples. Instead, this phenomenon can be explained from the fact that higher temperatures and concentrations lead to higher oxygen concentration and lower organic content in the TiO2.<sup>[21]</sup> A higher concentration of oxygen translates to a lower electron affinity and a higher band gap,<sup>[22]</sup> leading to a higher barrier for electron injection from Al to Si and, therefore, less current. Even a 0.1 eV increase in the barrier height can change the current by almost two orders of magnitude because  $\exp(-0.1q/kT)$  (assuming a thermionic emission model). This means that the change in barrier height that produces the changes between the lowest and the highest curves in Figure 4 is of order 0.1 eV. One must also note that the thickness and dielectric constant of the oxide may be different for different deposition conditions,<sup>[23,24]</sup> changing



**Figure 4.** *J*–V curves of Al/TiO<sub>2</sub>/n-Si structures for different deposition conditions. In the legend, C is the organometallic precursor concentration and  $T_a$  is the annealing temperature.

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**Figure 5.** Photoconductive effect for Al/TiO<sub>2</sub>/n-Si structures. This particular sample was produced with concentration of 0.15 M and annealing temperature of 540 °C. The inset shows the same plot in linear scale.

the value of *K*. In particular, for the deposition at concentration of 0.15 M and annealing temperature of 540 °C a slight linear increase of the "truncated current" as a function of voltage is observed. We suppose this is a consequence of a higher *K* value obtained for this film. This increase in *K* results in a square-root dependence of the voltage drop in titania with respect to the applied voltage (dashed lines of Figure 2), but since the SCLC mechanism gives a square-law J-V dependence, the resulting behavior is approximately linear, as observed.

The structure also presented a photoconductive effect, as shown in Figure 5. Here light is absorbed solely by Si, because the absorption edge of  $TiO_2$  is at about 390 nm (gap is  $\approx\!\!3.2\,eV^{[25]}\!)$  and the lamp we used in the photoconductance experiments was an incandescent lamp that produced only  $\approx 2 \,\mathrm{mW}\,\mathrm{cm}^{-2}$  of irradiance at the sample. The J–V response is only affected by light in the saturation part. This is because before saturation there is no depletion region to separate electrons and holes created by light. Instead, the photoelectrons and holes recombine before they can be collected by the terminals and constitute a photocurrent. On the other hand, once the flatband voltage is reached, a depletion region starts to set in, carriers begin to be separated and a photocurrent is created. We also note that when light is present the "saturation" current increases with increasing voltage (see the inset of Figure 5). This can also be easily accounted by our model. For increasing voltage, the depletion region width grows and more photoelectrons and holes are collected, giving more photocurrent. Because strong inversion is never reached, the depletion region keeps growing indefinitely as long as the voltage is increased. These effects further confirm our model.

In conclusion, we have shown that  $Al/TiO_2/n$ -Si structures behave differently than regular metal-oxide-semiconductor capacitors in two ways: first, there is a current saturation phenomenon associated with a transition of the semiconductor surface from accumulation to depletion and, second, the very high leakage current causes the structure to go into deep depletion instead of into strong inversion. We suggest that this may have interesting applications as a current source and as a light/particle detector. It is very inexpensive and extremely simple to fabricate. Further work is necessary to determine the performance of such devices.

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## Conflict of Interest

The authors declare no conflict of interest.

## **Keywords**

current saturation, semiconductor physics, space-charge-limited current,  $\mathrm{TiO}_{2}$ 

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