

# Cz Bifacial Solar Cells

C. del Cañizo, A. Moehlecke, I. Zanesco, and A. Luque

**Abstract**—High efficiencies have been achieved on bifacial solar cells made on FZ silicon. In the adaptation of the process to the more commonly used Cz material, attention has been paid to the influence of thermal processing on Cz, trying to avoid internal gettering effects related to oxygen precipitation. Lifetime measurements at different steps of the process have been carried out to quantify this influence. Reduction of “thermal load” by growth of a thin passivating oxide and deposition of a double antireflecting coating gives 17.7% when illuminated from the  $n^+$  side and 15.2% when illuminated from the  $p^+$  one.

**Index Terms**—Bifacial, Cz silicon, solar cells.

THERE has been much improvement in the last few years on bifacial solar cells. In 1994, a  $p^+nn^+$  structure developed at our laboratory reached 19.1% for  $n^+$  side illumination and 18.1% for  $p^+$  side illumination [1]. Hübner *et al.* [2] develop a cell passivated with silicon nitride and with local Al BSF in the rear side, giving 20.1% for front side illumination and 17.2% for rear side illumination. Glunz *et al.* [3] report for a rear contact cell an efficiency of 20.6% when illuminated by the unmetallized side, and 20.2% when illuminated by the metallized one. Also with a rear contact cell, Zhou *et al.* [4] achieve 20.6%-15.2% for a 10% coverage on the side with the contacts, and 21.9%-13.9% for 20% coverage. With screen printed contacts, best results reported are those of Rohatgi *et al.* [5], 16.4% front efficiency and 11.6% rear efficiency.

These results are always on high quality FZ material, while there is an interest in Cz silicon for industrial processes. The purpose of this paper is to report the development of a bifacial cell process for Cz Si.

To explain the modifications that lead to Cz cells, we analyze briefly our baseline process to obtain  $p^+nn^+$  or  $n^+pp^+$  bifacial cells [1], [6]. First, a masking oxide is grown to define the active area and to shield the  $n^+$  face from boron diffusion. Then, a texturization is done in a KOH bath, obtaining pyramid heights of around 3  $\mu\text{m}$ . Boron is diffused from a  $\text{BBr}_3$  source and another masking oxide is grown with same functions as the first one: to mask the  $p^+$  face from phosphorus diffusion and to define the  $n^+$  active area. The  $n^+$  side is texturized, and a phosphorus diffusion is carried out from a  $\text{POCl}_3$  source in supersaturation conditions, producing a gettering effect that recovers lifetime degraded by thermal processing. An etch-back step in

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C. del Cañizo and A. Luque are with the Instituto de Energía Solar, Universidad Politécnica de Madrid ETSI Telecomunicación, Ciudad Universitaria, s/n. 28040, Madrid, Spain (e-mail: canizo@ies-def.upm.es).

A. Moehlecke and I. Zanesco are with the Faculdade de Física, Pontifícia Universidade Católica do Rio Grande do Sul Avda. CEP 90619-900, Porto Alegre, RS, Brazil (e-mail: moehlecke@music.pucrs.br).

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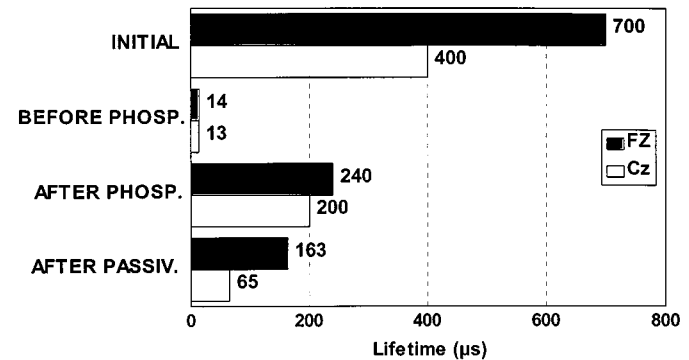


Fig. 1. Bulk lifetime evolution for FZ and Cz 20  $\Omega\text{-cm}$  n-type wafers for standard process.

a  $\text{HF}/\text{HNO}_3$  solution etches away the dead layer. After oxide etching in a buffered HF solution, a thick oxide (about 1000  $\text{\AA}$ ) is grown to passivate the surfaces and reduce reflection losses. Passivation of boron doped surfaces, which is known to be less effective than for phosphorus doped ones, is improved by implementation of a floating junction; we perform this floating junction passivation by a simple method, consisting of carrying out passivation oxidation step in a furnace for phosphorus diffusion. Metallization comprises evaporation of Ti-Pd-Ag on the  $n^+$  face and Al-Ti-Pd-Ag on the  $p^+$  face. Silver is electroplated to obtain 6–8  $\mu\text{m}$  high fingers. To improve metal adherence and recover surfaces damaged by electron-gun x-rays, an annealing in forming gas at 450  $^\circ\text{C}$  is performed as a last fabrication step.

We study the changes needed to adapt the process to Cz material by lifetime measurements and cell processing. The main difference between FZ and Cz is the fact that Cz silicon is rich in oxygen (concentration around  $10^{17}\text{--}10^{18}$   $\text{atm}/\text{cm}^3$ ), and thermal steps induce oxygen precipitation in the bulk, producing intrinsic gettering [7], which is detrimental for solar cell performance. However, there is not an agreement in how to avoid this phenomenon, and while some authors found that lifetime degradation in Cz is avoided by using only a single furnace step above 800  $^\circ\text{C}$  [8], others point out that high temperatures do not degrade lifetime provided fast ramping-up and ramping-down is performed [9]. In any case, it seems to be necessary to reduce the “thermal load” that Cz material is exposed to during processing.

To analyze the influence of thermal steps, we measured bulk lifetime after each thermal step for both FZ and Cz. Measurements are made with photoconductive decay technique (PCD). We etch the first few microns of the samples with CP4 to eliminate the diffused layers, and passivate the samples by immersion in HF 50% during the measurements. In Fig. 1, lifetime evolution for 20  $\Omega\text{-cm}$  n-type FZ and Cz samples is presented. Similar results have been obtained for p-type samples.

Lifetime is severely degraded by contamination during oxidations and boron deposition, because conventional furnaces

TABLE I  
RESULTS FROM A BIFACIAL Cz CELL WITH  
100 Å OXIDE + DARC, n TYPE, 20 Ωcm, 4 cm<sup>2</sup> (CONFIRMED BY NREL)

	$J_{sc}$ (mA/cm <sup>2</sup> )	$V_{oc}$ (mV)	FF	$\eta$ (%)
Illumination from n <sup>+</sup> side	36.32	613	0.796	17.7
Illumination from p <sup>+</sup> side	31.60	609	0.788	15.2

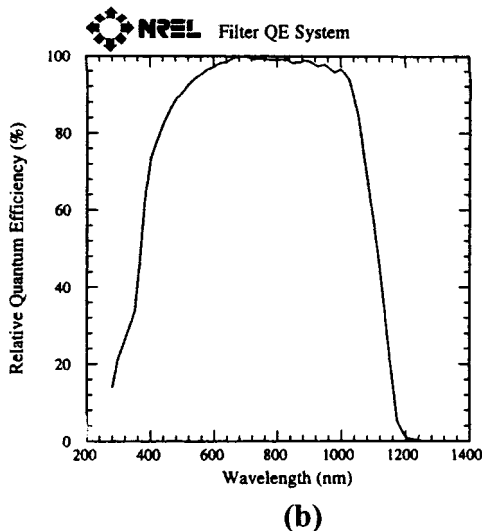
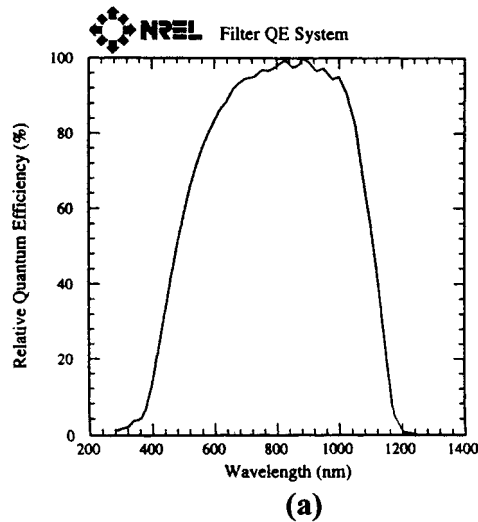


Fig. 2. Quantum efficiency of n-type Cz bifacial cell. (a) p<sup>+</sup> illumination; (b) n<sup>+</sup> illumination.

without TCA cleaning are used. A clear recovery due to phosphorus gettering is observed for both FZ and Cz (from around 15 μs to around 200 μs), but then the passivation step again reduces lifetime, and there the degradation is worse for Cz (that falls down to around 50 μs) than for FZ silicon (that stays at around 150 μs). PCID simulations indicate this lifetime reduction will decrease dramatically cell performance (for example,  $V_{oc}$  decreases 5%,  $J_{sc}$  at the p<sup>+</sup>n junction 2% and  $J_{sc}$  at the n<sup>+</sup>n junction 13%).

This analysis suggests that modifications on the passivation step should be developed, so that lifetime recovered during get-

tering step is not reduced as much by the oxidation. Then, we processed wafers where the last oxidation (1000 °C and around 90 min) is substituted by a process at 850 °C of around 45 min. This produces a thin oxide (around 100 Å) that passivates the surface but cannot perform as an anti-reflecting coating (ARC), so that a double ARC (ZnS and MgF<sub>2</sub>) is deposited after metallization.

Lifetime measurements after this short passivation step give 180 μs for Cz, which compared to measurements for the long process (around 50 μs) shows a clear improvement. This modification also affects floating junction formation, giving a higher sheet resistance, which is beneficial for surface recombination reduction [10]. Sheet resistance measured on test samples (wafers without any prior diffusion) is around 1000 Ω/□.

Table I shows cell parameters for a Cz cell, and Fig. 2 shows the quantum efficiency. Measurements have been made at NREL.

Poorer response in p<sup>+</sup> emitter is attributed to surface boron depletion. An extra-step to etch back this boron depleted layer can be performed to overcome this problem, allowing similar good short wavelength response for both illumination modes [6].

In conclusion, reduction of temperature and time of oxide-passivation step has succeeded in avoiding lifetime degradation, keeping base lifetime rather high. Cell performance is then limited by p<sup>+</sup> surface recombination, caused by boron depletion, which can be improved performing an extra boron etch-back step, or making boron diffusion as one of the last processing steps (before passivating oxide growth), in case phosphorus gettering is not needed.

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